Design Example Report

Title	***45 W Multi Output Flyback Converter with Two CV and One CC Using InnoMux™ IMX111U and InnoSwitch™ 3-MX INN3468C***
Specification	90 VAC – 265 VAC Input; 5 V / 1 A, 12 V / 1.25 A and 40 V / 0.65 A Outputs
Application	LED TV
Author	Applications Engineering Department
Document Number	DER-635
Date	August 12, 2021
Revision	3.2

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Summary and Features

Unique single-stage conversion, multiple-output, Flyback architecture enabling:

- High efficiency across the universal line range
- Energy Star 8.0 efficiency compliance
- High-accuracy, independently regulated 5 V / 1 A and 12 V / 1.25 A CV outputs with extremely fast load transient response of 150 µs and 250 µs respectively.
- One CC LED output with wide string voltage range of 30 V to 50 V suitable for wide range of television applications
- Configurable for
    - Analog dimming mode
    - Straight PWM dimming mode
    - Filtered PWM dimming mode and
    - Hybrid dimming mode.

InnoSwitch3-MX and InnoMux form an industry first AC/DC chipset with isolated, safety-rated integrated feedback. In addition there is built-in synchronous rectification for >90% efficiency at nominal AC input.

The control chipset incorporates isolated feedback and communication channels while implementing all the benefits of secondary-side control with the simplicity of primary-side regulation.

There are a few important safety features such as

- Output overvoltage protection (OVP), which eliminates the need for a fault protection optocoupler
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

The new architecture goals are to achieve tight cross regulation across multiple outputs and high overall efficiency while simplifying the overall system by removing conventional DC-DC converter post-regulation stages. This single-stage converterreduces board size significantly and shrinks part count about 50% compared to conventional converters that require extra converters. In addition to this high level of integration, benefits extend to InnoSwitch protection features such as input and output over/under-voltage and short-circuit protection.

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a PSU for an LED TV. This Switch Mode Power Supply (SMPS), utilizes the InnoSwitch3-MX and InnoMux from the InnoSwitch family. It has 5 V / 1 A and 12 V / 1.25 A outputs and a 25 W output providing power to one CC driver intended for the LED backlight in the TV panel. The total current through the LED strings is controlled from 0mA to 650mA by an analog signal (ADIM) with a full scale of 1.5 V. The total maximum power output is 45W, and the input voltage range is 90 VAC to 265 VAC.

The new architecture uses a multiplexed system with only one transformer as shown in Figure 1. For each switching cycle, the energy stored in the transformer during the primary conduction interval is delivered to only one of the converter's main outputs (CV1, CV2 or LED). Leveraging only a single magnetic component, the controller directs the energy flow as needed to all outputs based on respective loading requirements, thus keeping each output accurately controlled. This multiplexing is achieved by gating the steering FET Q2 or Q4 appropriately. If the energy pulse needs to be delivered to the CV1 output, Q2 is turned ON prior to the end of the primary conduction interval. Similarly, for CV2, the Q4 steering FET is used; otherwise if Q1 and Q4 are held OFF, the energy is delivered to the LED output via the rectification diode D3.

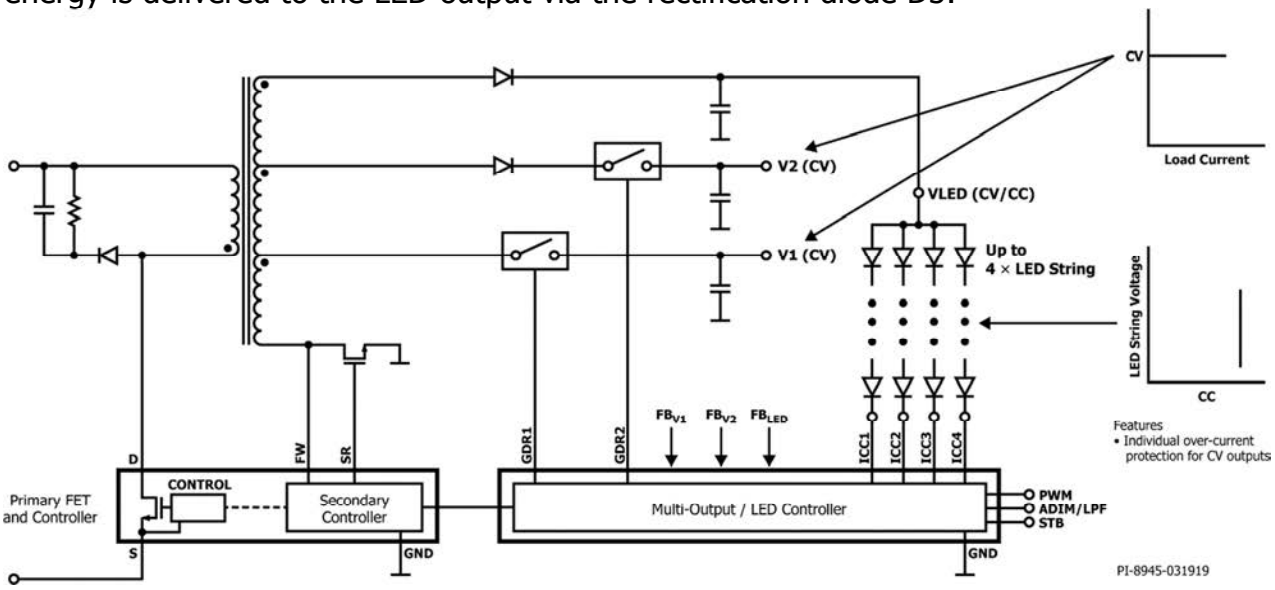


Figure 1 – DER-635 High Level Schematic.

The FB pins sense the output voltage and if needed (i.e. the voltage of one of the outputs is too low), the InnoMux IC sets the request pin to get one more pulse from the InnoSwitch3-MX IC. Every pulse given by the InnoSwitch3-MX IC is followed by an acknowledge pulse to the InnoMux IC. After that, the pulse energy is transferred to the secondary side and the InnoMux IC can adjust the energy setting as explained above. This method enables pulse-by-pulse regulation resulting in quick response and great cross regulation. For the described multiplexing algorithm to work correctly, it is essential that the transformer turns ratios are chosen such that the minimum LED output voltage reflected to the primary of the transformer is greater than the CV output voltage reflected to the transformer primary. This technique achieves cross regulation within a fraction of 1% while significantly improving system efficiency when compared to conventional post-regulation architectures. The new architecture supports multiple outputs driving both constant current and constant voltage loads, enabling the design of a single switch-mode power conversion stage that powers logic circuitry, USB ports, audio channels, and LED strings simultaneously.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

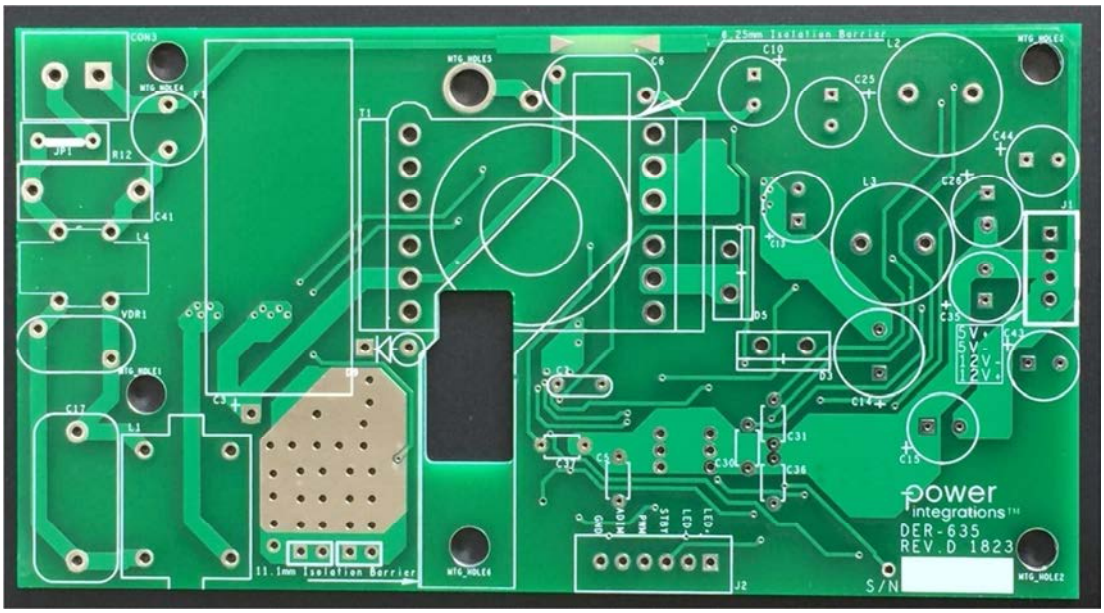


Figure 2 – PCB, Top View.

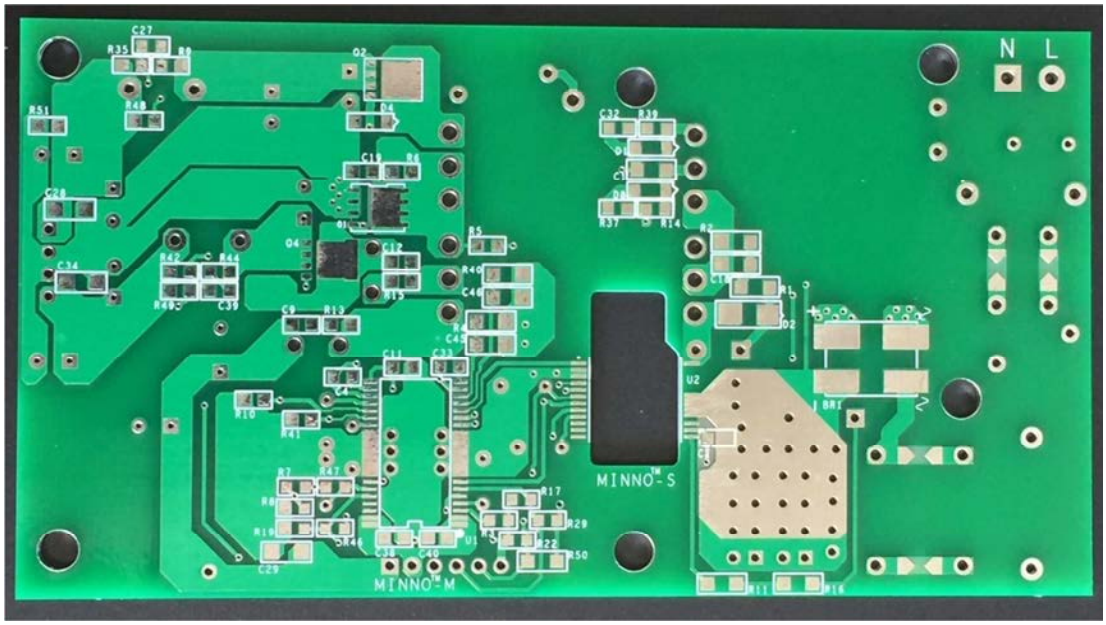


Figure 3 – PCB, Bottom View.

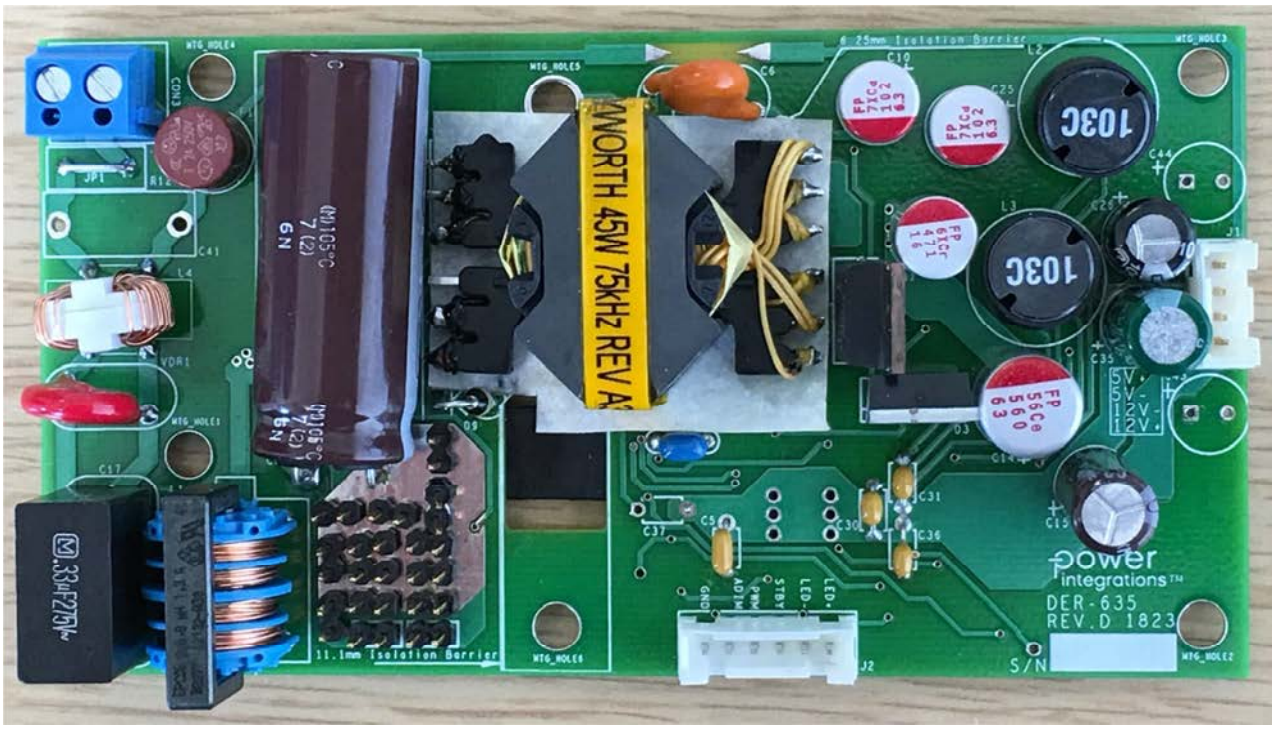


Figure 4 – PCB assembly, Top View.

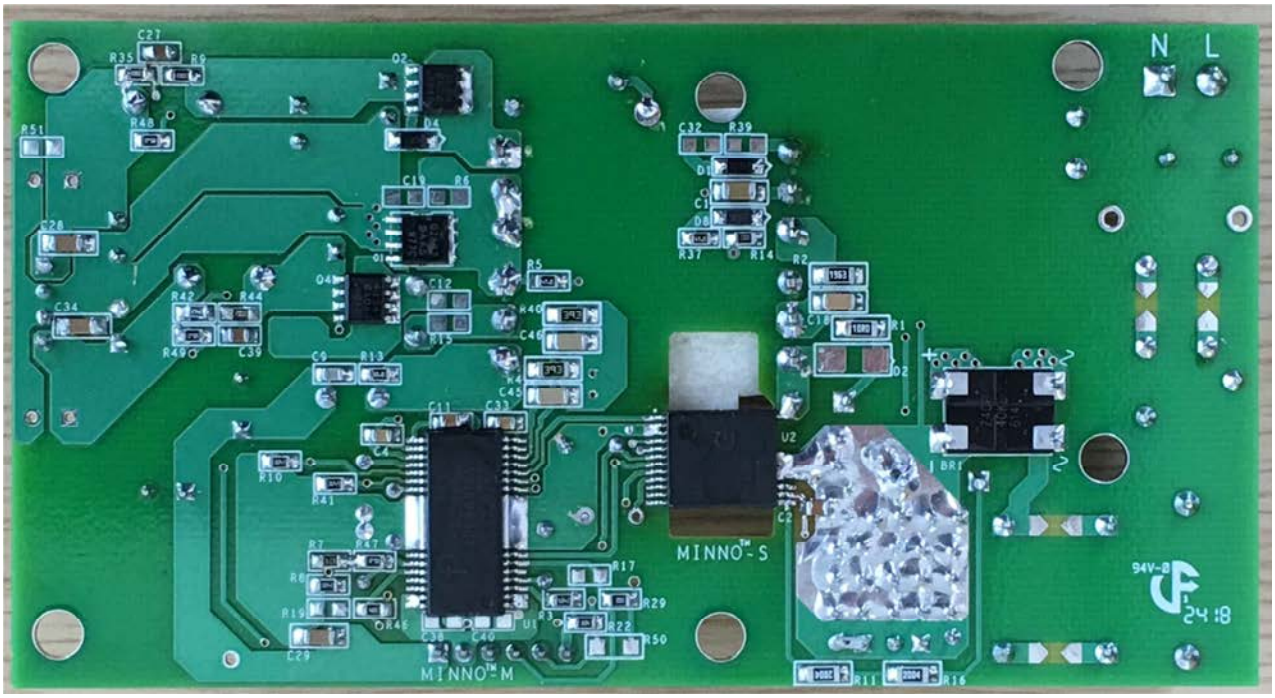


Figure 5 – PCB assembly, Bottom View.

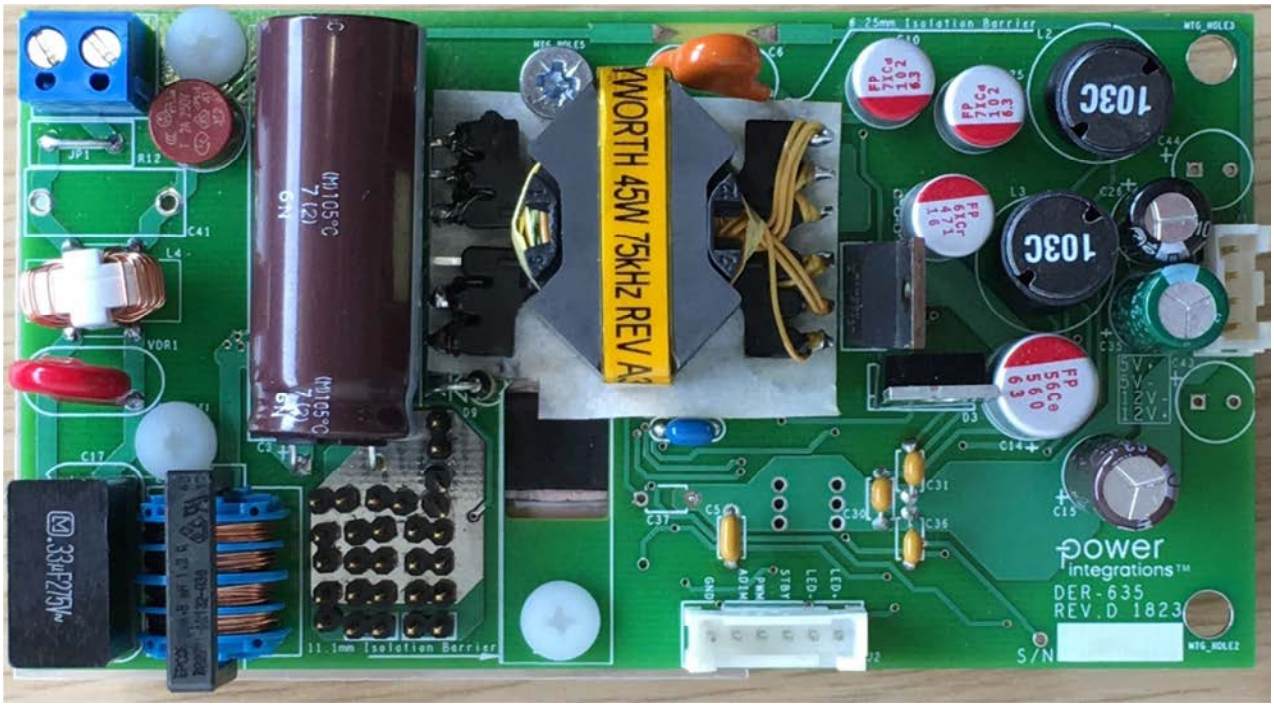


Figure 6 – Cooling Assembly, Top View.

Figure 7 – Cooling Assembly, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5%.
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0		1	A	
Output Voltage 2	V_{OUT2}	11.4	12	12.6	V	±5%.
Output Ripple Voltage 2	$V_{RIPPLE2}$			100	mV	20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0		1.25	A	
Output Voltage 3	V_{OUT3}	30	40	50	V	
Output Ripple Current 3	$I_{RIPPLE3}$			60	mA	20 MHz Bandwidth.
Output Current 3	I_{OUT3}	0	0.6	0.65		
Total Output Power						
Continuous Output Power	P_{OUT}			45	W	
Efficiency						
Full Load	η	87			%	Measured at 110 / 230 VAC, P_{OUT} 25 ºC.
No-Load Input Power				0.27	W	Measured at 230 VAC 25 ºC, 5 V 20 mA, 11 Pin Pulled Low.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Common Mode Ring Wave		4		6	kV	100 kHz Ring Wave, 12 Ω Common Mode.
Surge Combination Wave				1	kV	Combination Wave, 2 Ω Differential Mode.
ESD		±2		±15	kV	Air Discharge.
		±2		±8		Contact Discharge.
Ambient Temperature	T_{AMB}	0		60	°C	Free Convection, Sea Level.

Table 1 – Power Supply Specification.

3 **Schematic**

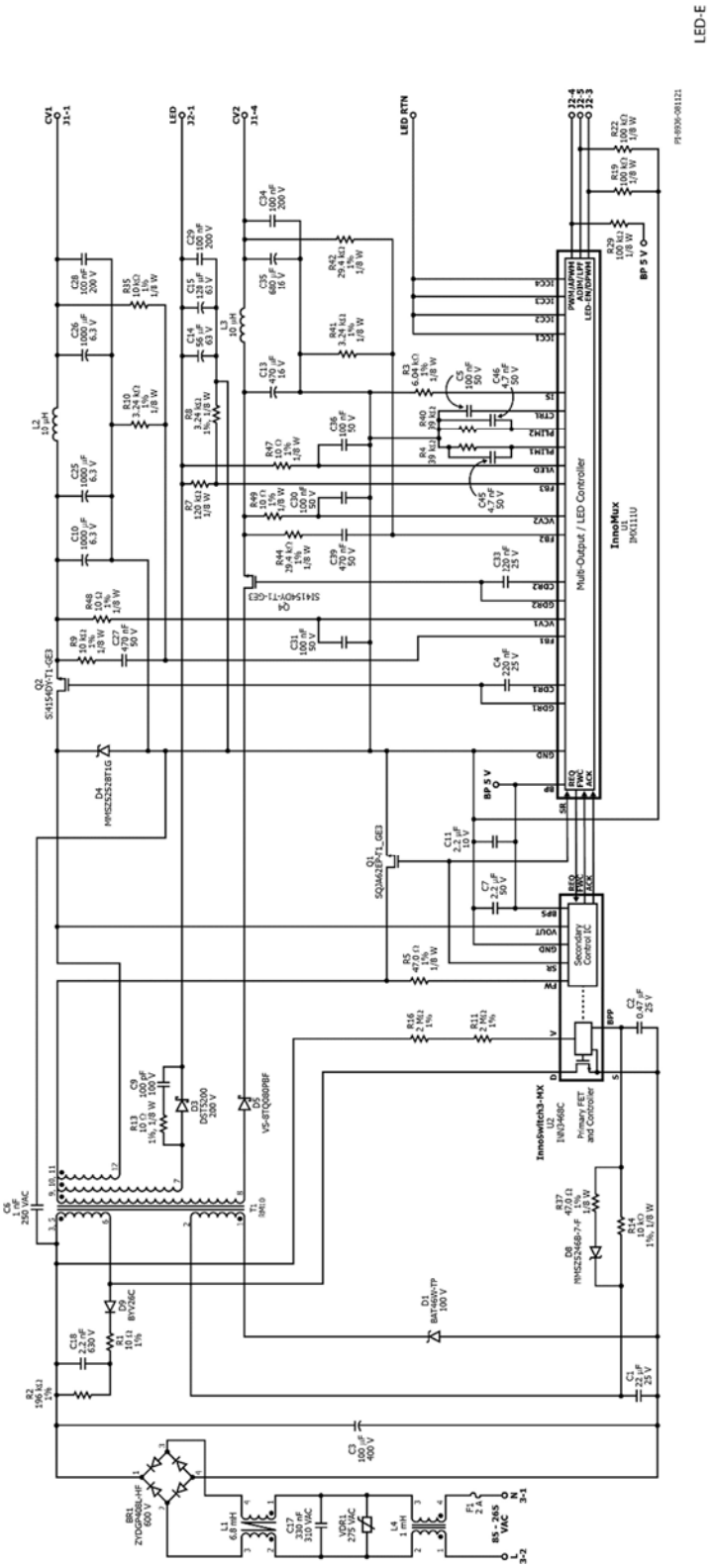


Figure 8 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

A two-stage EMI filter is used on the line AC input, C17/L1 for lower frequencies and L4 for high frequencies. Mainly common mode noise is suppressed by the input filter, but useful suppression of differential noise is also achieved. These measures along with the Y capacitor C6 and screen windings in the transformer keep the conducted emissions below the specification limits.

The bulk storage capacitor C3 provides DC voltage smoothing after the bridge rectifier BR1. VDR1 provides protection against differential voltage surges, andF1 protects the system from any kind of failure.

4.2 *Primary-Side*

See data sheet for InnoSwitch3-MX operation details

The transformer primary is connected between the rectified DC bus (VIN_DC_TX) and the drain of an integrated power MOSFET within the InnoSwitch3-MX (U2 pin 24). Primary current is returned to the bulk capacitor (C3) via the source tab of U2 (pin 16).

A low cost RCD clamp, formed by D2, R1, R2 and C18, limits the peak drain voltage due to the effects of transformer leakage inductance and output trace inductance.

4.2.1 Primary-Side Controller Power Source and OVP Protection

The primary-side IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C2, when AC is first applied. During normal operation the primary side of the controller is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D1 and capacitor C1, and fed into the BPP pin via a current limiting resistor R14.

4.2.2 Primary-Side OVP, Brown-In and Brown-Out Protection

The primary-side output overvoltage protection is obtained using Zener diode D8. In the event of an uncontrolled overvoltage at the output, the increased voltage at the bias winding causes the zener diode D8 to conduct and trigger the OVP protection in the primary-side controller.

Resistor R16 and R11 provide line voltage sensing to provide controlled brown-in/out thresholds. These are set to approximately 75 VAC and 65 VAC respectively. At approximately 320 VAC, the current through these resistors exceeds the over overvoltage threshold, which results in the disabling of U2.

4.2.3 Primary Peak Current Limit

Capacitor C2 is 0.47 μF which sets the primary-side controller peak current to 'Standard' i.e. 2.2 A.

4.3 ***Secondary-Side***

See latest data sheet for InnoMux operation details

The secondary-side of the InnoSwitch3-MX (U2) is powered by the BP pin of the InnoMux IC (U1 pin 15) and decoupled by C7.

4.3.1 Primary to Secondary-side Communication

The secondary-side of the InnoSwitch3-MX (U2) requests the primary-side to initiate a switching cycle via the FluxLink, a galvanically isolated control channel. This occurs when the InnoMux (U1) raises the REQ pin (U2 pin 1) to the appropriate level.

4.3.2 Synchronous Rectifier (SR) FET Control

The gate of the SR FET (Q1) is turned on based on the winding voltage sensed via R5 and the FW pin (U2 pin 9). In continuous conduction mode operation, the SR FET (Q1) is turned off just prior to the secondary-side controller requesting a new switching cycle from the primary. In discontinuous current mode (DCM), the SR FET (Q1) is turned off when the voltage drop across the Q1 falls below a threshold ($V_{SR(TH)}$). Secondary-side control of the primary-side MOSFET ensures that the primary-side power MOSFET and SR FET are never turned on simultaneously. The SR FET gate drive signal (U2 pin 7) has an amplitude of 5 V. Consequently, a logic level MOSFET must be used as a SR.

4.3.3 InnoSwitch3-MX to InnoMux Communication

Communication between InnoSwitch3-MX (U2) and InnoMux (U1) is executed through the following:

REQ (request) pin – this is an analog multi-level input with the following thresholds:

- <0.3 V – InnoMux is in reset
- 0.3 V - 0.61 V – InnoMux is in idle ring measurement window mode
- 0.61 V - 1.22 V – no pulse requested, but has control
- 1.22 V - 2.44 V – pulse requested
- >2.44 V – error, output over-voltage. Primary will latched off

ACK (acknowledge) pin – On recognition of the switching cycle request from the InnoMux IC (U1), the InnoSwitch3-MX (U2) secondary side sends an acknowledge pulse to the InnoMux IC (U1). This is a digital signal.

The SR pin is used to drive the SR FET and informs the InnoMux IC (U1) when the transformer is delivering energy to the secondary circuit.

FWC (forward) pin – this is an indication of the total secondary discharge time. This is a digital signal from the InnoSwitch3-MX IC (U2) to the InnoMux IC (U1). Similar to the SR signal, this signal indicates the discharge time more completely, as the SR may be turned off early.

4.3.4 InnoMux power sources

See latest data sheet for InnoMux operation details

The InnoMux secondary-side control IC is powered by +V_LED during start-up via R47 and C36 (optional extra ESD suppression) and VLED (U1 pin 23). An internal regulator reduces this to 5 V and outputs it on BP (U1 pin15). C11 provides BP5V decoupling for U1. The BP pin output powers the secondary-side controller of the InnoSwitch3-MX IC.

Once the voltage on VCV2 (U1 pin 21) reaches $VCV2_{MIN}$ (5.8 V to 8.0 V) the regulator input is switched from VLED to VCV2 to conserve power. VLED may be up to 100 V whereas VCV2 is set to 12 V, the less voltage dropped, the lower the power loss. Resistor R49 and C30 provide optional extra ESD suppression.

4.3.5 High Side MOSFET Driver for Q2 or Q4

The gate drive to the selection MOSFETs Q2 and Q4 provides a 5 V drive so a logic level MOSFET must be used. Capacitors C4 and C33 are charged up to the level of +V_CV1, 5 V and +V_CV2, 5 V respectively, resulting in the capacitors being raised by 5 V, the BP level, to generate the 5 V gate drive pulse to the steering MOSFETs.

To allow visibility of the idle ring to the FW pin, Q2 is held on after a CV1/2/VLED discharge cycle to permit Quasi-resonant Switching when in DCM mode. During this time the InnoMux IC will send a REQ for the next pulse. When an ACK is received, Q2 is turned off.

4.3.6 Output Control

Output rectification for the 5 V output is provided by the SR FET (Q1) and the CV1 selection MOSFET (Q2). Very low ESR capacitors, C10 and C25, provide filtering, and inductor L2 and capacitors C26 and C28 form a second-stage filter that significantly attenuates the high frequency ripple and noise at the 5 V output.

Output rectification for the 12 V output is provided by the SR FET (Q1) and the CV2 selection MOSFET (Q4) and CV2 diode (D5). Very low ESR capacitor, C13, provide filtering, and inductor L3 and capacitors C35 and C34 form a second-stage filter that significantly attenuates the high frequency ripple and noise at the 12 V output.

Output rectification for the LED output is provided by SR FET (Q1) and diode (D3). Very low ESR capacitors, C14 and C15, provide energy storage and filtering at the LED output.

The RC snubber network comprising R13 and C9 for D3 damps high-frequency ringing across the diode, which results from leakage inductance of the transformer windings and the secondary's trace inductances.

Zener diode D4 is used as a voltage clamp for the transformer CV1 winding while the primary MOSFET is ON and Q1, Q2 and Q4 are turned off, and D5, D3 are reverse biased. In this condition, the secondary windings are floating with respect to GND. Without D4, the voltage on Q2 drain could be too high due to transformer winding capacitance interactions.

When the selection MOSFET (Q2) and the SR FET (Q1) are turned on, the transformer secondary windings are designed such that the voltage on the anode of D3 or D5 is below the lowest working LED string voltage and 12 V respectively. Therefore D3 and D5 will remain reverse biased and all the transformer energy is directed to the CV1 output via Q1.

When the Selection MOSFET (Q2) is turned off and the Selection MOSFET (Q4) and SR FET (Q1) is turned on, the voltage on the anode of D3 is below the lowest working LED string voltage, keeping the diode reverse biased. In this condition all the transformer energy is directed to the 12 V output.

When the Selection MOSFETs (Q2 and Q4) are turned off, and the SR FET (Q2) is turned on, the voltage on the anode of D3 rises until it is forward biased. In this condition, all the transformer energy is directed to the LED output.

+V_CV1 output voltage is set by R35 and R10 to FB1 (U1 pin 19). Loop compensation is provided by R9 and C27 due to the inclusion of L2.

+V_CV2 output voltage is set by R41 and R42 to FB2 (U1 pin 20). Loop compensation is provided by R44 and C38 due to the inclusion of L3.

+V_LED output overvoltage limit is set by R7 and R8 to FB3 (U1 pin 22). For DER-635 it has been set to 55 V.

Note: The actual +V_LED voltage is not set by these resistors; it is set by the voltage drop across the LED drivers ICC1-4, which is dependent on LED string current.

4.3.7 LED Current Control and Dimming

The LED current per driver is set by R3 on IS (U1 pin 3) plus, for this application which is configured for analog dimming, the voltage on ADIM (U1 pin 5). The resistance on the IS pin sets the maximum LED current per driver at the maximum ADIM voltage of 1.5 V. DER-635 has been set up for 650 mA total through 4 drivers (162 mA per driver) with 1.5 V on ADIM.

Other dimming options are available, such as PWM, Sequenced PWM and combinations of Analog and PWM. It is simple to re-configure DER-635 to another dimming method. *See latest data sheet for InnoMux operation details.*

4.3.8 Output Power Limits

The maximum power delivered to each output of the converter is limited by the maximum frequency at which this output can receive pulses of energy from the transformer primary. These limits are set by the values of the components connected to the PLIM1 and the PLIM2 pin. Four discrete protection levels are available for each output. (For details, see Table 3 and Table 4 in the InnoMUX datasheets.). The power limits on the CV1 output and the LED output are set by the values of resistors R4 and R40 respectively (Figure 8). The power limit on the CV2 output is set by the presence or the absence of capacitors between pins PLIM1 and PWM2 and GND (C45 and C46 in Figure 8). The controller implements auto-restart sequence if the maximum frequency on any output exceeds the set maximum value for a predetermined time interval.

4.3.9 Standby Mode

The LED-EN pin is held at GND by R19, so the InnoMux IC is in 'Standby Mode'. Here, the LED driver circuit is powered down, reducing the InnoMux power requirement and the +V_LED output is maintained at a level of at least 15 V. With a standby load of 100 mW on +V_CV1, a standby power at 230 VAC of under 300 mW can be realized. If the STBY pin rises too high (3.3 V to 5 V), the LED would be activated and would enter normal run mode.

While in Standby Mode, full rated power (5 W) is still available on the +V_CV1 output and full rated power (15 W) on the +V_CV2 output.

4.3.10 Start-Up Process

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 8
Pri FET Vds [V]	CV1 5V Output [V]	V led Output [V]	BP5V [V]	U1/2 REQ pin [V]	U1/2 ACK pin [V]	LED Output Current [A]

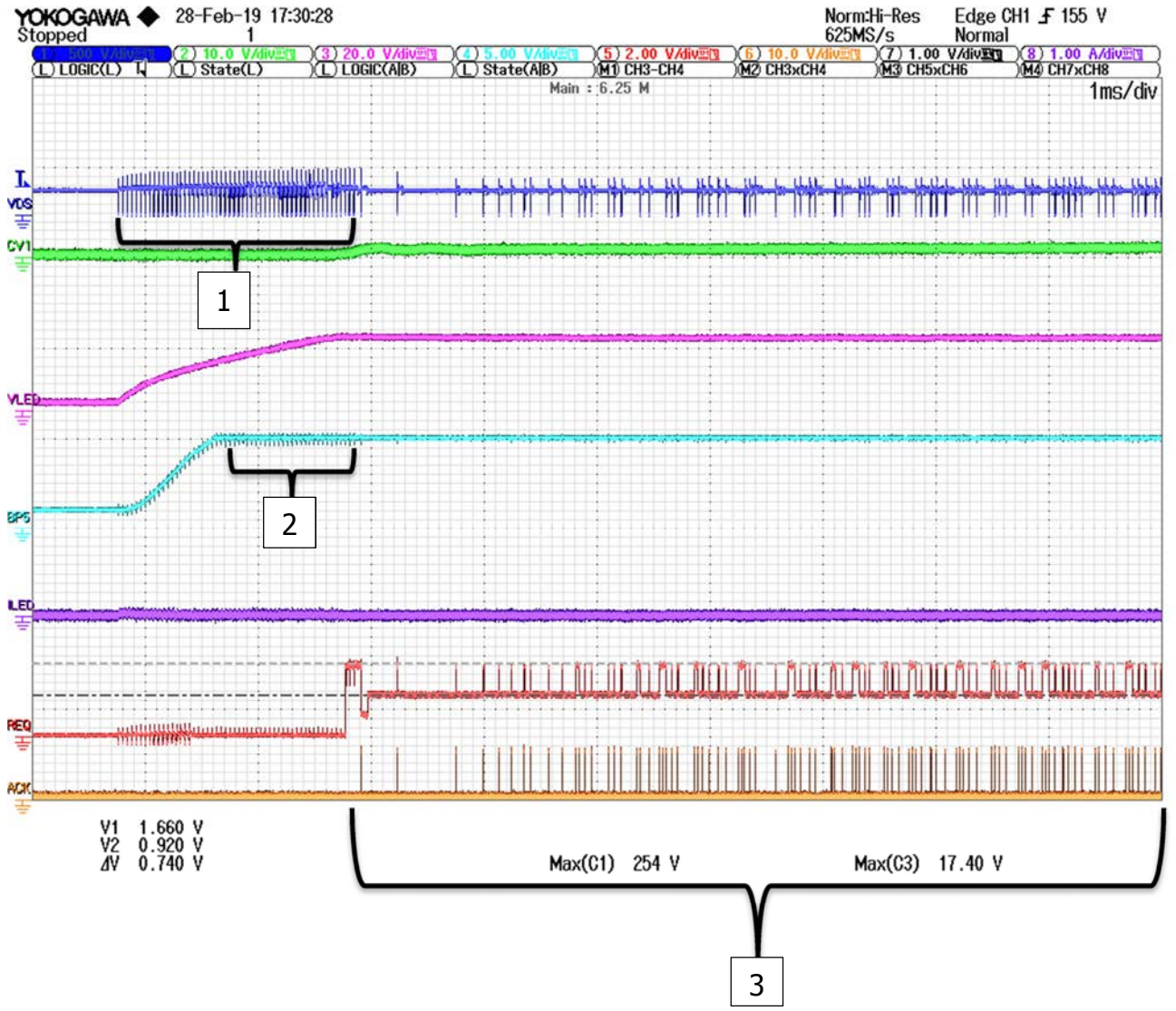


Figure 9 – First 10 ms of Start-Up.

1. Secondary-side controllers are un-powered or initializing, so the primary-side controller switches without feedback information at a default rate of about 25 kHz, and peak current is set to approximately 75% of the maximum level. If the secondary side is unresponsive, the primary side will time out and shut down, or the primary-side bias voltage will rise enough to trigger a bias OVP shutdown.
2. The LED output is the only output to rise significantly during period [1]. Eventually it will rise to a level where the InnoMux (U1) internal series regulator can establish 5 V on BP5V. At this point, U1 is drawing power only from the LED output via the VLED pin (pin 23). U2 is powered by U1 via the BP pin (U1 pin15). U1 and U2 secondary-side controllers then initialize, and U1 raises the REQ pin (U1 pin 10) to request a pulse from the primary-side controller (~1.7 V).
3. When the InnoSwitch3-MX secondary-side recognizes the signal, it requests a pulse from the primary side and outputs an acknowledge pulse on the ACK pin (U2 pin 4). When the InnoMux IC (U2) recognizes the ACK signal, it drops the REQ pin to the 'No Pulse Request' level (~0.9 V). The InnoMux IC (U2) then uses Q2 or Q4 to direct a proportion of the flyback pulses to the CV1 or CV2 respectively and the rest to the LED output.
4. CV1, CV2, and LED output voltages can be seen to rise somewhat together. At some time during period 4, the CV2 will reach a sufficient level to power U1 and U2 via the VCV2 pin (U1 pin 21). The U2 regulator will automatically switch to drawing power only via the VCV2 pin, which is a more efficient source.

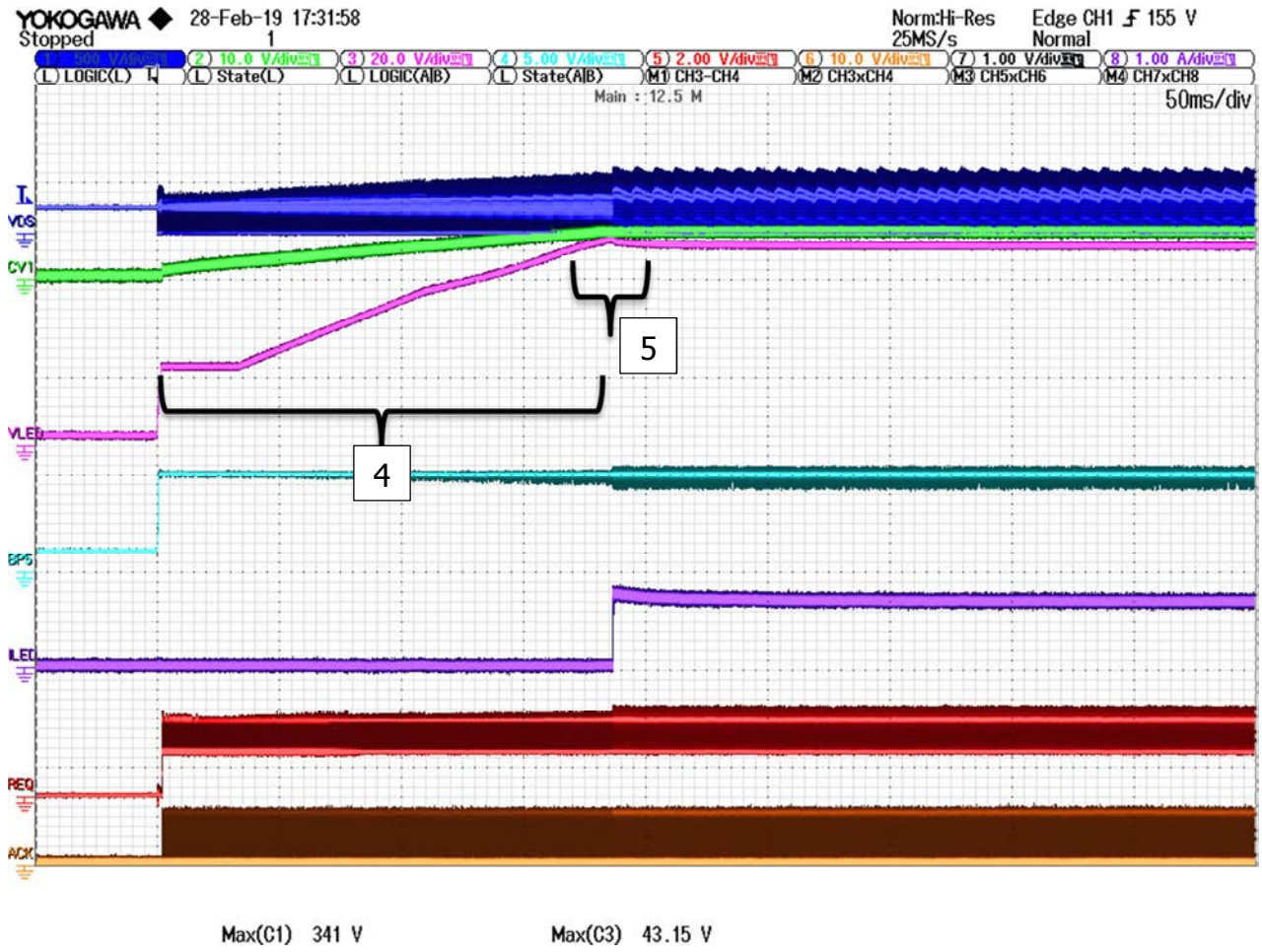


Figure 10 – Complete Start-Up Cycle Over Approximately 230 ms**.**

5. As the LED output voltage rises, a point will be reached when the forward voltage drop of the LED strings will be exceeded, causing the voltage across the LED drivers (U2 pins 1, 2, 27, and 28) to rise. This is detected by the InnoMux controller, and the drivers are turned on, in a sequence, to determine how many parallel LED strings are attached (always all four in DER-635 which has only one LED string – shorting all these pins). If in standby, this causes the LEDs to flash very briefly. In normal operating mode, the LED current through each string is regulated to the level set by the voltage on the ADIM pin (U1 pin 5).

5 DER-635 Connection Diagram

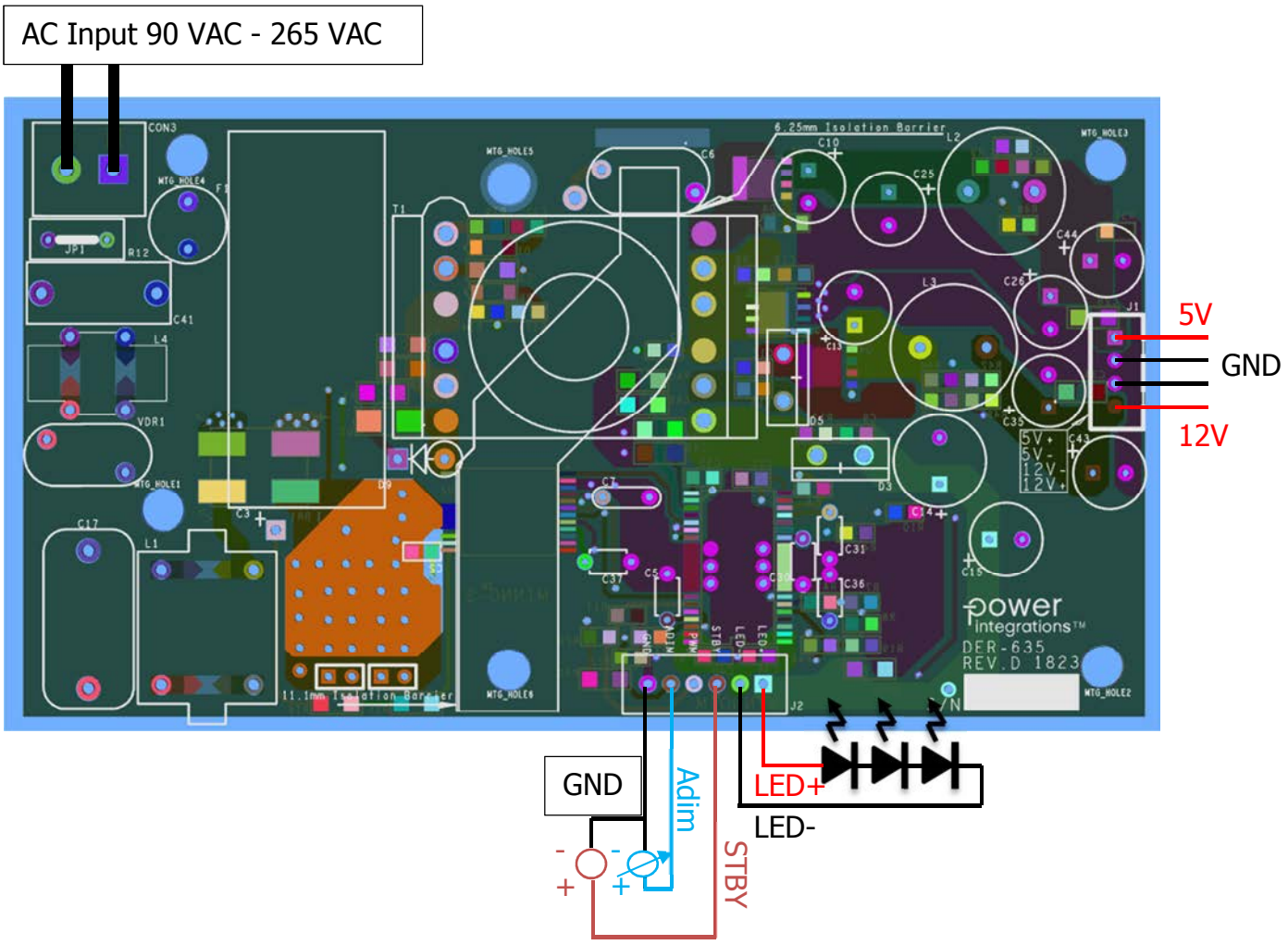


Figure 11 – DER-635 Connection Diagram.

6 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 μm) unless otherwise stated

To minimize crosstalk between the outputs of the converter, it is advisable to minimize the length of the connection between the negative terminals of C10 and C25 to the source of SR (Q1). The same applies to the connection from the negative terminals of C14 and C15 or C13 to the source of SR (Q1). The three AC paths to the SR source should be kept separate.

Ideally the connection between the GND pins of U1 and U2 should not be shared with any AC ripple current in the output filter stages. This is important for achieving accurate synchronous rectification.

The primary switch in InnoSwitch3-MX IC is cooled through the SOURCE pin (the paddle) of the IC. Care should be taken that the thermal impedance between the paddle and the cooling copper of the PCB is kept to a minimum. For best results the cooling copper pour should flair out as rapidly as possible away from the solder joint.

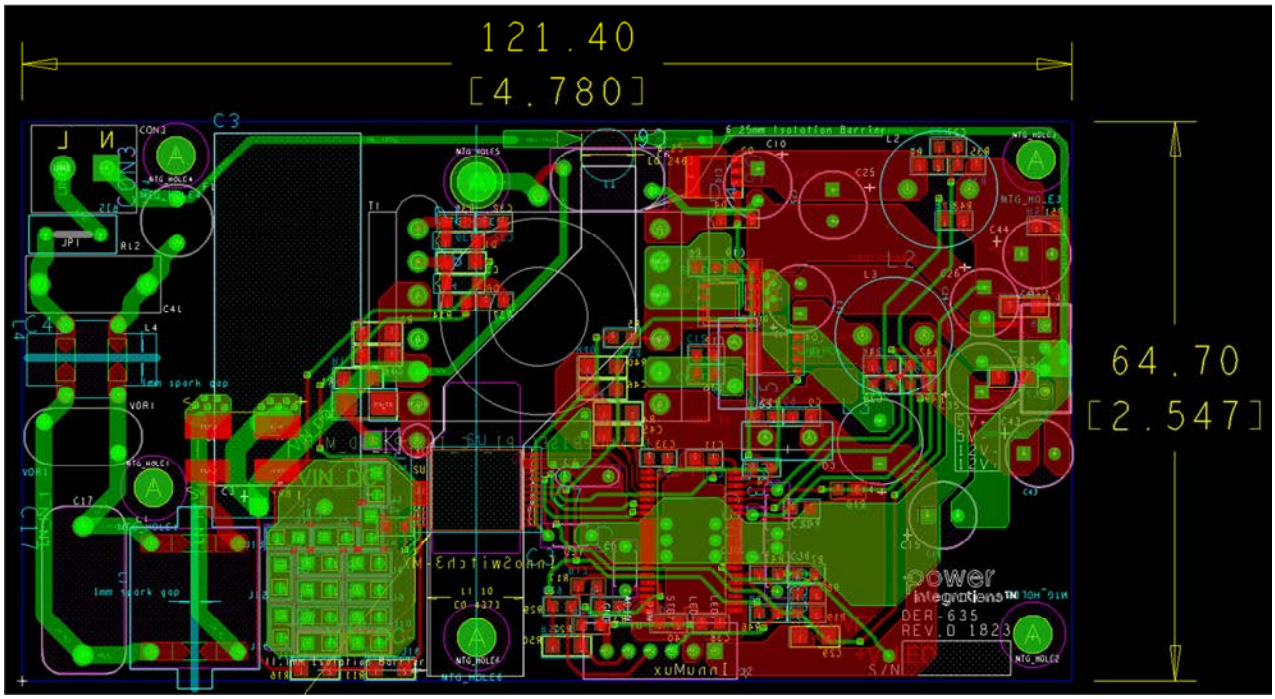


Figure 12 – Printed Circuit Layout.

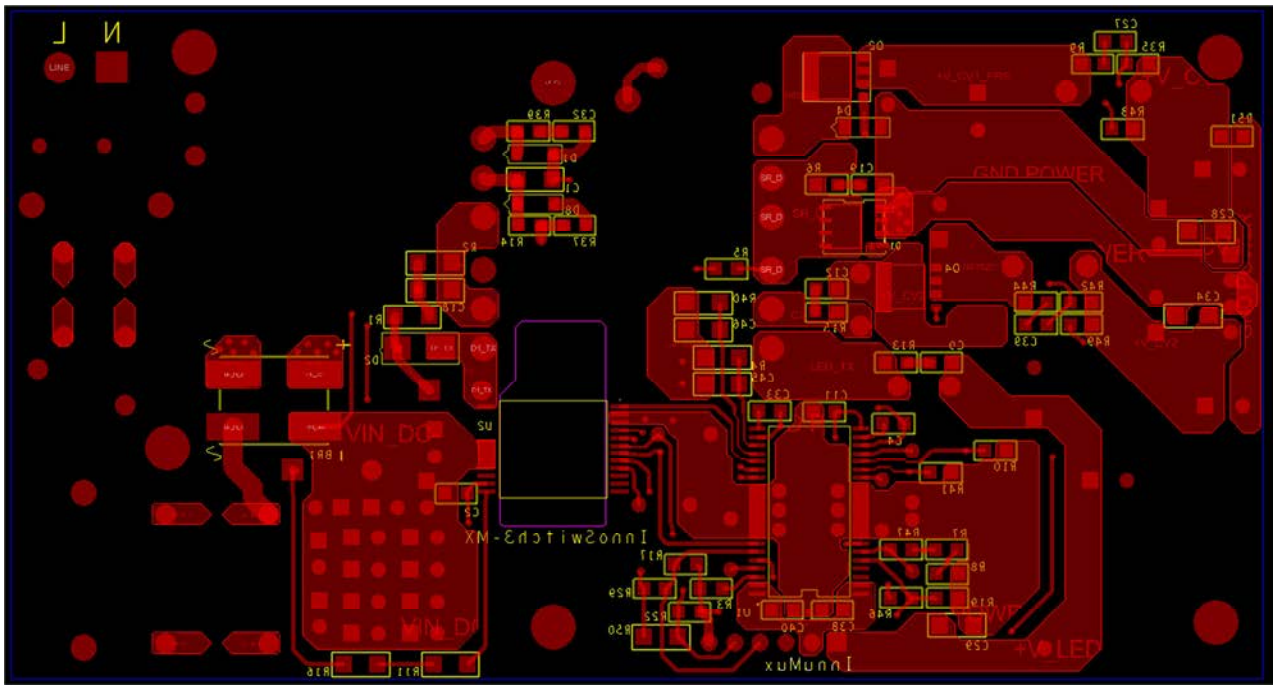


Figure 13 – Printed Circuit Layout, Bottom.

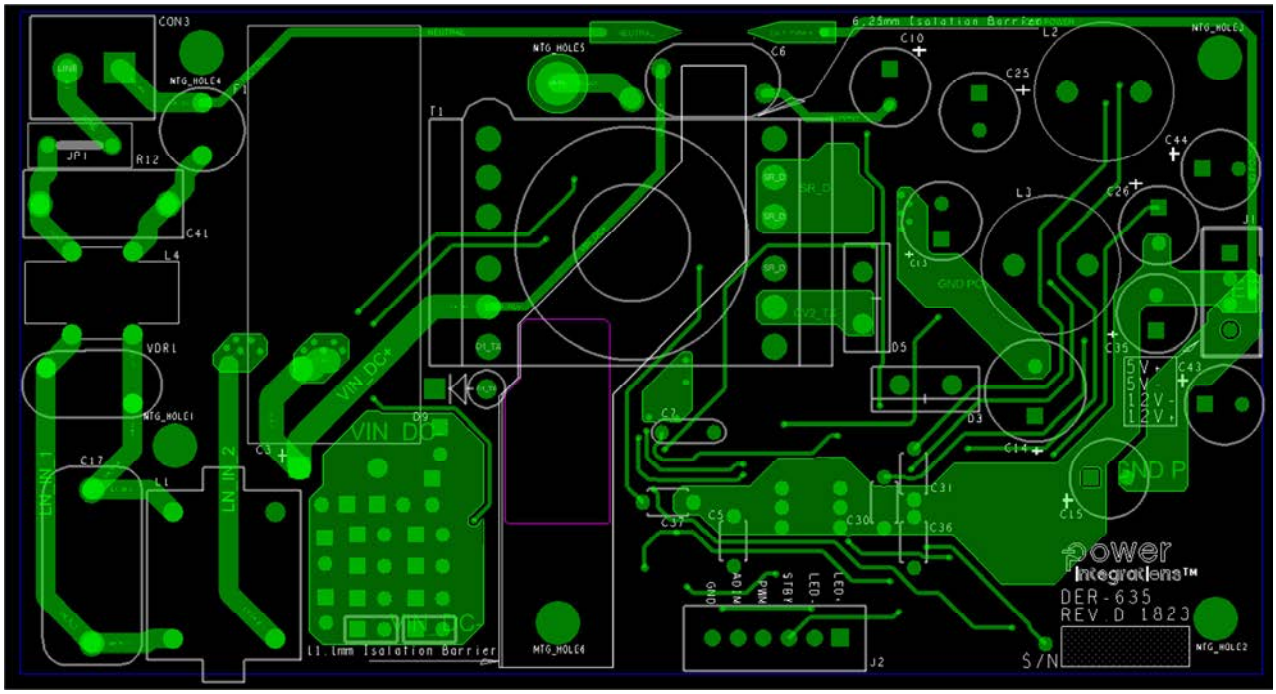


Figure 14 – Printed Circuit Layout, Top.

7 Bill of Materials

The total number of items in DER-635 is 54 with a total of 78 parts.

Item	Ref Des	Qty	Description	Mfg Part Number	Mfg
1	BR1	1	RECT BRIDGE, GP, 800 V, 4 A, Z4-D	Z4DGP408L-HF	Comchip
2	C1	1	22 µF, 25 V, Ceramic, X5R, 1206	CL31A226KAHNNNE	Murata
3	C10 C25	2	1000 µF, 20%, 6.3 V, Al Organic Polymer, Gen. Purpose, 2000 Hrs @ 105 °C, (8 x 8 mm)	RL80J102MDN1KX	Nichicon
4	C11	1	2.2 µF, 10 V, Ceramic, X7R, 0805	C0805C225M8RACTU	Kemet
5	C13	1	470 µF, 16 V,Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
6	C14	1	56 µF, ±20%, 63 V, Aluminum Polymer Electrolytic, 25 mΩ, -55°C ~ 105°C, 2000 Hrs @ 105°C, (10 x 14)	RNU1J560MDN1PH	Nichicon
7	C15	1	120 µF, ±20%, 63 V, Aluminum Electrolytic, Radial, Can 3000 Hrs @ 105°C (8 x 21.5mm)	EKZE630EC3121MH20D	United Chemi-con
8	C17	1	330 nF, 275 VAC, Film, X2	ECQ-U2A334ML	Panasonic
9	C18	1	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
10	C2	1	0.47 µF CER 25 V X7R 0805	CGA4J2X7R1E474K125AA	TDK
11	C26	1	1000 µF, 6.3 V, Electrolytic, Gen Purpose, (8 x 11.5)	ECA-0JHG102	Panasonic
12	C27 C39	2	470 nF, 50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Murata
13	C28 C29 C34	3	100 nF, 200 V, Ceramic, X7R, 1206	VJ1206Y104KXCAT	Vishay
14	C3	1	100 µF, 400 V, Electrolytic, Low ESR, 630 mΩ, (16 x 40)	EKMX401ELL101ML40S	Nippon Chemi-Con
15	C35	1	680 µF, 16 V, Electrolytic, Very Low ESR, 38 mΩ, (8 x 20)	EKZE160ELL681MH20D	Nippon Chemi-Con
16	C4 C33	2	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
17	C45 C46	2	4.7 nF, 50 V, Ceramic, X7R, 1206	CC1206KRX7R9BB472	Yageo
18	C5 C30 C31 C36	4	100 nF, 50 V, Ceramic, X7R	K104K15X7RF5TH5	Vishay BC Components
19	C6	1	1 nF, Ceramic, Y1	440LD10-R	Vishay
20	C7	1	2.2 µF, 50 V, Ceramic, X7R	FG24X7R1H225KRT06	TDK
21	C9	1	100 pF 100 V 10 % X7R 0805	08051C101JAT2A	AVX
22	CON3	1	CONN TERM BLOCK 5.08 mm 2POS	ED120/2DS	On Shore Tech
23	D1	1	Diode, Schottky, 100 V, 0.075 A, SOD123	BAT46W-TP	Micro Commercial
24	D3	1	200 V, 5 A, Diode, Schottky, Fast Recovery =< 500 ns, > 200 mA (Io), -55°C ~ 150 °C, TO-220AC	DST5200	Littlefuse
25	D4	1	Diode Zener 24 V 500 mW SOD123	MMSZ5252BT1G	ON Semi
26	D5	1	80 V, 8 A, Diode, Schottky, Fast Recovery =< 500 ns, > 200 mA (Io), -55°C ~ 175°C, TO-220AC	VS-8TQ100-M3	Vishay
27	D8	1	Diode Zener 16 V 500 mW SOD123	MMSZ5246B-7-F	Diodes, Inc.
28	D9	1	600 V, 1 A, Ultrafast Recovery, 30 ns, SOD57	BYV26C	Philips
29	F1	1	2 A, 250 V, Slow, TR5	37212000411	Wickman
30	J1	1	4 Positions (1 x 4) Header, Shrouded, 0.098" (2.50 mm,) Through Hole, Gold,0.177" (4.50 mm) mating length	DF1B-4P-2.5DSA(01)	Hirose Electric
31	J2	1	6 Position (1 x 6) header, 2.5 mm pitch, Vertical	DF1B-6P-2.5DSA(01)	Hirose Electric
32	JP1	1	Wire Jumper, Non-insulated, #20 AWG, 0.2 in	8020 000100	Belden
33	L1	1	CMC, 6.8 mH @ 10kHz, 1.3A,2 Line, DCR 280 mΩ (Typ), -40°C ~ 125°C, Through Hole	B82731M2132A030	Epcos
34	L2 L3	2	10 µH, Unshielded Wirewound Inductor, 3.45 A, 15 m Ω Max, Radial, Vertical Cylinder	18R103C	Murata
35	L4	1	1 mH @ 100 kHz, 2 A, 80 mΩ, 250 V, -25°C ~ 105°C, CMC	SC-02-10GS	KEMET
36	Q1	1	MOSFET, N-Channel, 60 V, 60 A (Tc), 68 W (Tc), PowerPAK® SO-8, PowerPAK SO-8	SQJA62EP-T1_GE3	Vishay
37	Q2 Q4	2	MOSFET,N-Channel, 40 V, 36 A (Tc), 3.5 W (Ta), 7.8 W (Tc), SMT, 8-SO	SI4154DY-T1-GE3	Vishay
38	R1	1	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic

39	R11 R16	2	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
40	R13 R47 R48 R49	4	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
41	R19 R22 R29	3	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
42	R2	1	RES, 196 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1963V	Panasonic
43	R3	1	RES, 6.04 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6041V	Panasonic
44	R4 R40	2	RES, 39 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ393V	Panasonic
45	R42 R44	2	RES, 29.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2942V	Panasonic
46	R5 R37	2	RES, 47.0 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
47	R51	1	RES, 4.99 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4991V	Panasonic
48	R7	1	RES, 120 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ124V	Panasonic
49	R8 R10 R41	3	RES, 3.24 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3241V	Panasonic
50	R9 R14 R35	3	RES, 10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
51	T1	1	Bobbin, RM10, Vertical, 12 pins	B65814C1512T001	TDK
52	U1	1	InnoMux IC	IMX111U	Power Integrations
53	U2	1	InnoSwitch3-MX IC	INN3468C	Power Integrations
54	VDR1	1	275 VAC, 45 J, 10 mm, RADIAL	V275LA10P	Littlefuse

9 PI Expert Design Tool output

Inno_MUX_Flyback_ 020119; Rev.1.1; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	Inno3-MX Flyback Design Spreadsheet
Power Supply Basic Parameters					
VAC MIN	90.00		90	V	Minimum input AC voltage
VAC NOM			115	V	Nom. AC voltage - universal designs low line
VAC MAX			265	V	Maximum input AC voltage
POUT			41.88	W	Total output power
`			45.00	W	Total maximum output power
LINEFREQ			50	Hz	Line frequency
VMIN			92.8	V	Minimum instantaneous DC input voltage at min mains
VMIN AVG			112.3	V	Average input voltage calculated at VAC MIN
OUT_NUM			3		Select number of outputs
DESIGN RESULT					Design result
Input Section					
CAP_INPUT	100.00		100.00	uF	Input capacitance
IAVG_PRIMARY			0.52	A	Average diode bridge current (DC input current)
Output 1 Specification					
VO	5.00		5.00	V	Output 1 voltage
IO	1.00		1.000	A	Output 1 current
VO_TOL	0.00		0.00	%	Output 1 voltage tolerance
EFFICIENCY			86.00	%	Converter efficiency for output 1
Z			60.00	%	Secondary loss allocation factor for output 1
CONN_TYPE	AC_STACK		AC_STACK		Winding connection type
Output 2 Specification					
VO	12.00		12.00	V	Output 2 voltage
IO	1.25		1.250	A	Output 2 current
VO_TOL	0.00		0.00	%	Output 2 voltage tolerance
EFFICIENCY			86.00	%	Converter efficiency for output 2
Z			60.00	%	Secondary loss allocation factor for output 2
CONN_TYPE	AC_STACK		AC_STACK		Winding connection type
Output 3 Specification					
VO			35	V	Output 3 voltage
IO	0.63		0.625	A	Output 3 current
VO_TOL	14.28		14.28	%	Output 3 voltage tolerance
EFFICIENCY			90	%	Converter efficiency for output 3
Z			50	%	Secondary loss allocation factor for output 3
CONN_TYPE			AC_STACK		Winding connection type
Other Design Conditions					
VOR_TARGET			109.33	V	Maximum reflected voltage target
KP_MIN	1.05		1.054		Min. Current continuity factor for highest voltage output
Device Parameters					
DEVNAME	INN3468		INN3468		PI device name
DEVICE_MODE	Standard		Standard		Device current limit Mode
ILIMITTYP			2.20	A	Typical current limit
VDRAIN_MAX	650.00		650	V	Main switch brake down voltage
Transformer Electrical Parameters					
LP_NOM			320.87	uH	Nominal primary inductance
LP_TOL	3.00		3.00	%	Primary inductance tolerance
NP			32	turns	Calculated primary winding total number of turns
BM			0.23	Tesla	Maximum flux density
BP			0.25	Tesla	Peak flux density
Transformer Mechanical Parameters					
CR_TYPE	RM10/I		RM10/I		Core type

BB_TYPE			RM10/I - ,(P6 + S6)		Bobbin type
AE	98.00		98.00	mm^2	Core cross section
BW			10.30	mm	Bobbin winding width
VE			4310	mm^3	Core volume
LG			0.363	mm	Estimated gap length
AL			4050	nH/Turn	Ungapped core specific inductance
ALG			313	nH/Turn	Gapped core specific inductance
Transformer Construction					
TURNS BIAS	4.00		4	turns	Turns primary bias
TURNS SEC BIAS				turns	Turns secondary bias
NP	32.00		32	Turns	Total number of primary turns
NP_SECT1			16	Turns	Primary first part - First winding section from the core
NP_SECT2			16	Turns	Primary second part - Third winding section from the core
NS1_STACK			3	turns	Output 1 number of Turns
NS1			3	turns	Sec. Winding 1 -Fourth winding section from the core
NS2_STACK			2	turns	Output 2 number of Turns
NS2	5.00		5	turns	Sec. winding 2 - Fifth winding section from the core
NS3_STACK			7	turns	Output 3 number of turns
NS3	12.00		12	turns	Sec. winding 3 - Second winding section from the core
Operating Parameters Worst case					
FS			87060	Hz	Maximum operating switching frequency
FS_MIN			54001	Hz	Minimum operating switching frequency
KRPKDP			0.64		Minimum current continuity factor
VOR_ACTUAL			109.33	V	Actual maximum reflected voltage
VOR_MARG_23MAX_ACT			0.76101		Maximum VOR margin between output 2 and 3 reflected voltage (3 Outputs Only)
DMAX			0.53		Maximum duty cycle (at VMIN and full load)
TON			7.90		Maximum controller ON time (at VMIN and full load)
TOFF			6.06		Minimum controller OFF time (at VMIN and full load)
VDRAIN			484	V	Off state drain to source voltage
VDS_ON			0.52	V	On state drain to source voltage
IP			2.24	A	Peak primary current (at VMIN and full load)
IRMS			0.90	A	Primary RMS current (at VMIN and full load)
ISRMS_STACK1			5.55	A	Secondary 1 winding RMS current
ISRMS_STACK2			3.79	A	Secondary 2 winding RMS current
ISRMS_STACK3			1.6086	A	Secondary 3 winding RMS current
PTRFLOSS_TOT			0.78	W	Total transformer power loss
PTRFLOSS_WIND			0.18	W	Transformer windings power loss
PTRFLOSS_CORE			0.60	W	Transformer core power loss
Output Parameters (Worst case)					
Output 1					
VO1			5.00	V	Output 1 voltage
IO1			1.00	A	Output 1 current
PO1			5.00	W	Output 1 power
PO1_MAX			5.00	W	Output 1 maximum power
VD1			0.40	V	Estimated forward voltage across output diode
KP1			0.64		Current continuity factor during output 1 conduction
DMAX1			0.38		Duty cycle during output 1 conduction
ISP1			23.84	A	Secondary peak current during output 1 Conduction
ISRMS1			4.05	A	Output 1 RMS current
IRIPPLE1			3.93	A	Output 1 capacitor - RMS ripple current
Output 1 Components					

VO1_RIPPLE	0.10		0.10	V	Output 1 ripple voltage
COUT1			1033.74	uF	Minimum output capacitance required
RESR1			0.05	R	Output 1 capacitor ESR value
COUT1_PLOSS			0.77	W	Output 1 capacitor ESR losses
VZ1			15.37	V	Minimum zener 1 clamp voltage
OSR1_PIVS			50.51	V	Synch. Rectifier 1 voltage
OSR1_RDSON			0.01	Ohm	Sync. Rectifier 1 ON resistance
OSF1_PLOSS			0.16	W	Sync. Rectifier 1 conduction Losses
OSF1_PIVS			15.37	V	Selection FET 1 minimum voltage
OSF1_RDSON			0.01	Ohm	Selection FET 1 ON resistance
OSF1_PLOSS			0.16	W	Selection FET 1 conduction losses
Output 2					
VO2			12.00	V	Output 2 voltage
IO2			1.25	A	Output 2 current
PO2			15.00	W	Output 2 power
PO2_MAX			15.00	W	Output 2 maximum power
VD2			1.00	V	Estimated forward voltage across output 2 diode/rectifier
KP2			0.89		Current continuity factor during output 2 conduction
DMAX2			0.47		Duty cycle during output 2 conduction
ISP2			14.22	A	Secondary peak current during output 2 conduction
ISRMS2			3.43	A	Output 2 RMS current
IRIPPLE2			3.19	A	Output 2 capacitor - RMS ripple current
Output 2 Components					
VO2_RIPPLE	0.10		0.10	V	Output 2 ripple voltage
COUT2			474.68	uF	Minimum output 2 capacitance required
RESR2			0.05	Ohm	Output 2 capacitor ESR value
COUT2_PLOSS			0.51	W	Output 2 capacitor ESR losses
OD2_PIVS			35.42	V	Output 2 diode voltage
OSF2_RDSON			0.01	Ohm	Selection FET 2 ON resistance
OSF2_PLOSS			0.11752	W	Selection FET 2 ON losses
OD2_PLOSS			1.25	W	Output diode 2 losses
Output 3					
VO3			35	V	Output 3 voltage
IO3			0.625	A	Output 3 current
PO3			21.875	W	Output 3 power
PO3_MAX			24.9988	W	Output 3 maximum power
VD3			1	V	Estimated forward voltage across output 2 diode
KP3			1.054		Current continuity factor during output 3 conduction
DMAX3			0.52927		Duty cycle during Output 3 conduction
ISP3			5.9254	A	Secondary peak current during output 3 conduction
ISRMS3			1.6086	A	Output 3 RMS current
IRIPPLE3			1.4822	A	Output 3 capacitor - RMS ripple current
Output 3 Components					
VO3_RIPPLE			0.1	V	Output 3 ripple voltage
COUT3			143.755	uF	Minimum output 3 capacitance required
RES3			0.05	Ohm	Output 3 capacitor ESR value
COUT3_PLOSS			0.10985	W	Output 3 capacitor ESR losses
OD3_PIVS			145.401	V	Output diode 3 voltage rating
OD3_VFD			1	V	Actual output diode 3 voltage drop
OD3_PLOSS			0.625	W	Output diode 3 losses
Bias Section					
NBIAS			4	turns	Primary bias winding turns
VB			12.00	V	Primary bias voltage
VF_BIAS			0.70	V	Primary bias voltage forward drop
VR_BIAS			58.85	V	Primary bias reverse voltage

CBIAS			22	uF	Primary bias capacitor
VBS				V	Secondary bias voltage
NBIAS_SEC				turns	Turns secondary bias
VF_BIASS				V	Secondary bias rectifier voltage forward drop
VR_BIASS				V	Secondary bias rectifier reverse voltage
Tolerance Analysis					
Output Index	1.00		1		Output to be displayed
VO1_VO2_VO3_Corner	nom-nom-nom		nom-nom-nom		VO tolerance corner to be displayed
ILIMIT_LP_Corner	nom-nom		nom-nom		Curr.Limit/Inductance combination to be displayed
VO			5.00	V	Actual output voltage
VOR			57.60	V	Reflected voltage
IO			1.00	A	Output current
PO			5.00	W	Actual output power
FS			66640.48	Hz	Switching frequency
DMAX			0.38		Duty cycle
KP			0.80		Current continuity factor
TON			5.68	us	Controller ON time
TOFF			9.33	us	Controller OFF time
IP1			2.10	A	Primary peak current
ISRMS			3.92	A	Secondary RMS current
IRIPPLE			3.79	A	Output capacitor - RMS ripple current
BM			2143.92	Gauss	Maximum flux density (Steady State Condition)
BP			2250.98	Gauss	Peak flux density (@ 132kHz - transitory condition)
IRMS @ VMIN AVG			0.752	A	Primary RMS current at VMIN AVG (VO1=Nom, VO2=Nom, VO3=Max) or (VO1=Nom, VO2=Max)
Errors, Warnings, Information					
Information					Although the design has passed the user should validate functionality on the bench. Please check the variables listed.
Design Warnings					Design variables whose values exceed electrical/datasheet specifications.
Design Errors					The list of design variables which result in an infeasible design.

Table 2 – PIxls Results.

10 Transformer (T1) Specification

10.1 *Core Information*

Core RM10, TDK Part No. PC47RM10Z-12

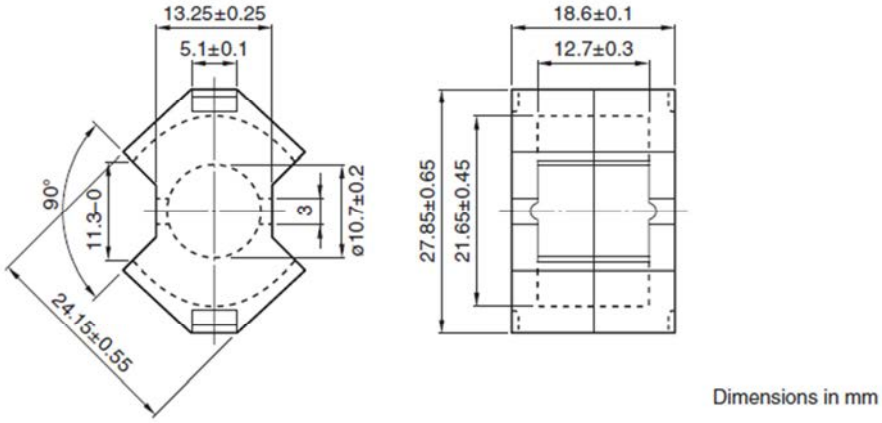


Figure 15 – *RM10 Core – geometry.*

Core Characteristics

Effective parameter								Electrical characteristics		
Core factor	Effective magnetic path length	Effective cross-sectional area	Effective core volume	Cross-sectional center pole area	Minimum cross-sectional center pole are	Cross-sectional winding area of core	Weigh	AL-value *		Core loss
C1	ℓe	Ae	Ve	Acp	Acp min.	Acw				
(mm−1)	(mm)	(mm2)	(mm3)	(mm2)	(mm2)	(mm2)	(g/set)	(nH/N2)		(W)max.
								1kHz 0.5mA	100kHz 200mT	100kHz 200mT 100°C
0.450	44.0	98.0	4310	89.9	86.6	69.5	23	4850±25%	7000 min.	1.70

Table 3 – Core Specification.

10.2 ***Bobbin Information***

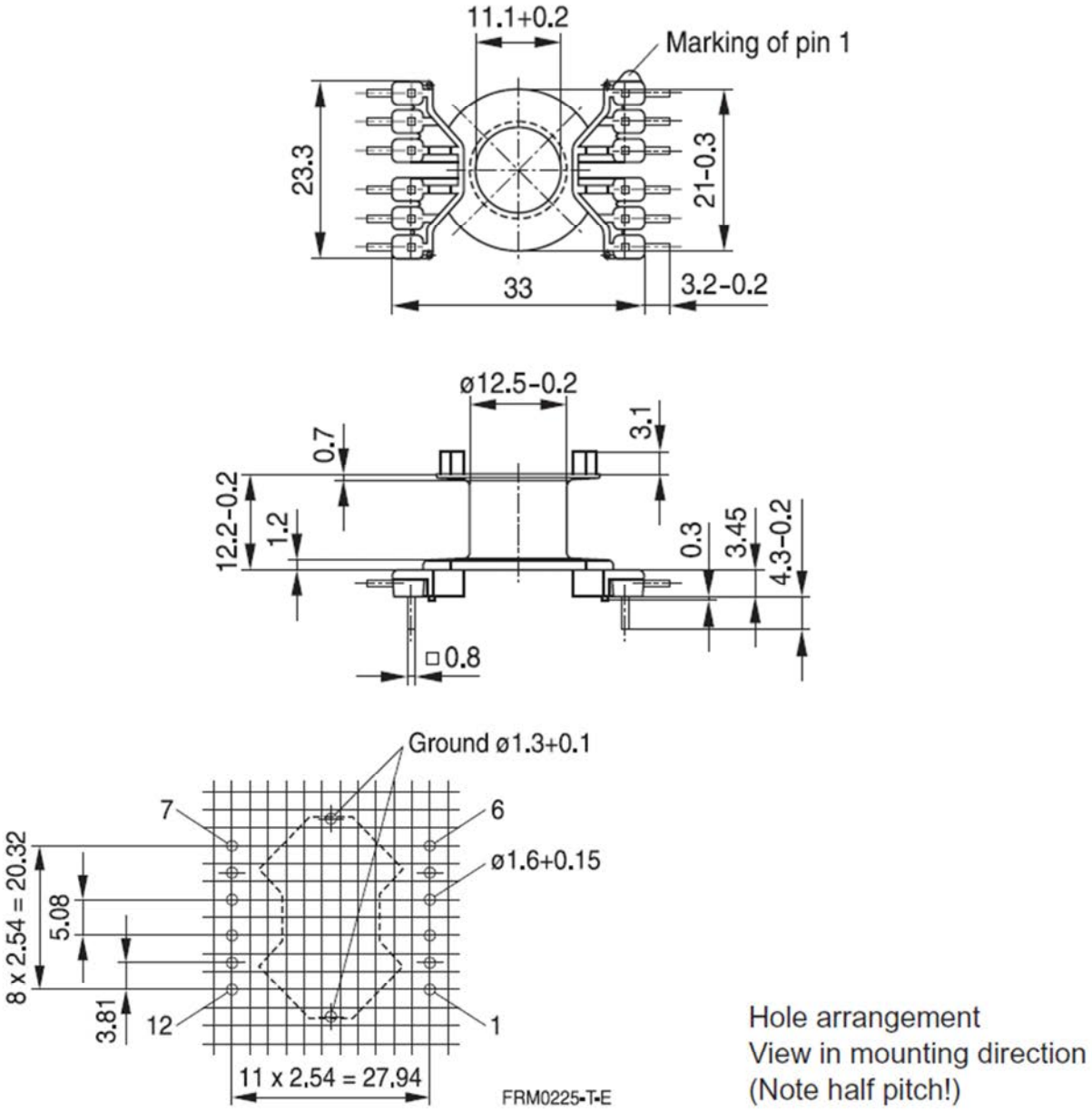


Figure 16 – TDK RM10 - 12 Pin Bobbin - B65814.

10.3 *Electrical Diagram*

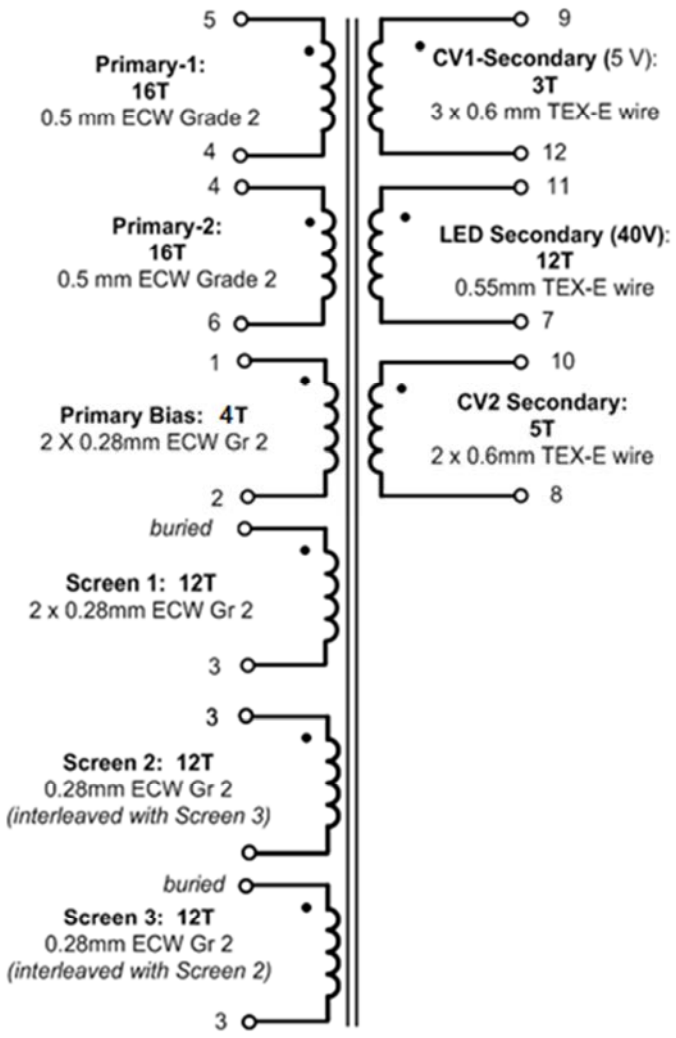


Figure 17 – Transformer Electrical Diagram.

10.4 *Winding Stack Diagram*

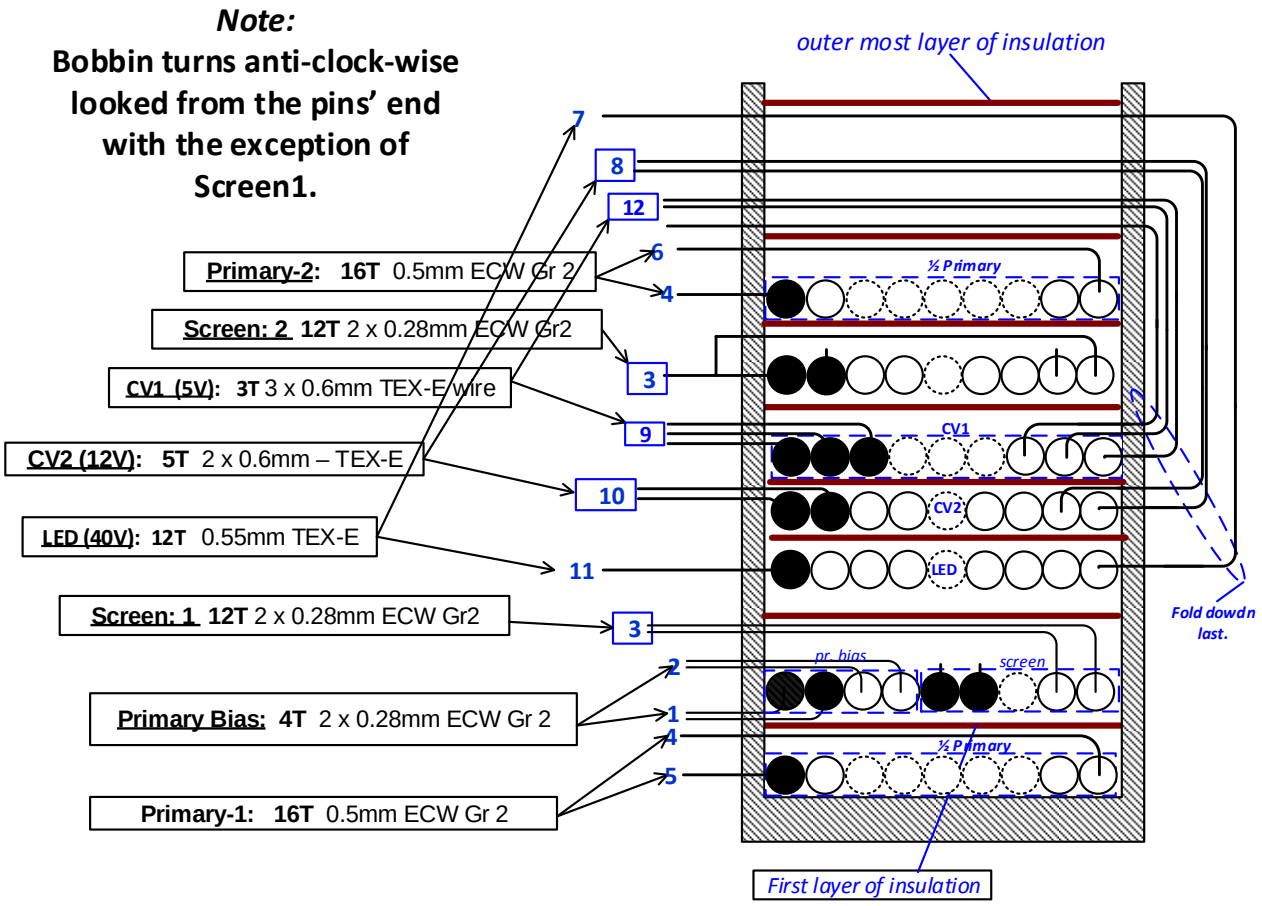


Figure 18 – Transformer Build Diagram.

10.5 *Electrical Specifications*

Parameter	Condition	Spec.
Electrical strength	1 second, 60 Hz from pins 1-6 to 7-1.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 4, with all other windings open.	320 µH ±3%
Resonant Frequency	Between pin 5 and 6, other windings open.	1,100 kHz (Min.)
Primary Leakage Inductance	Between pin 5 and 6, with all secondary 7, 8, 9, 10, 11 and 12 shorted.	3 µH (Max.)

Table 4 – Transformer Electrical Specification.

10.6 *Materials List*

Item	Description	Quantities
[1]	Core: RM10 TDK Part No. PC47RM10Z-12.	2
[2]	Bobbin: RM10-12 Pins; TDK, PI#: 25-01132-00.	1
[3]	Magnet Wire: 0.28 mm ECW Gr 2.	30 cm
[4]	Magnet Wire: 0.5 mm ECW Gr 2.	20 cm
[5]	Magnet Wire: 0.55 mm, Triple Insulated Wire.	10 cm
[6]	Magnet Wire: 0.6 mm, Triple Insulated Wire.	20 cm
[7]	Barrier Tape: Polyester Film, 1 mil thickness, 10 mm Wide.	10 cm
[8]	Clamps: RM10 TDK Part No. B65814.	2
[9]	Varnish: MR8008B - Varnish, Insulating, Polyurethane, Transparent/Amber EMR8008B250ML Or BC-359 https://www.eis-inc.com/medias/sys_master/ha9/h32/8797299081246.pdf	5 ml

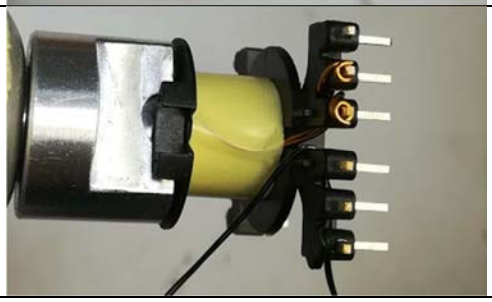
Table 5 – Transformer BOM.

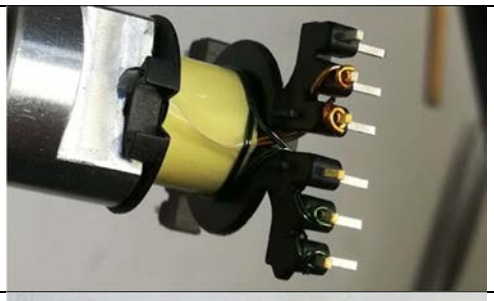
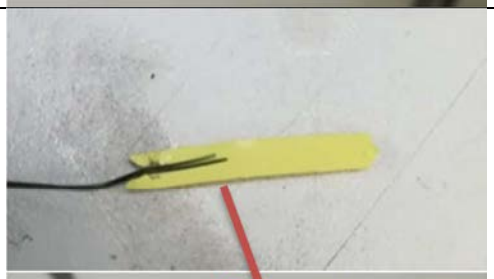
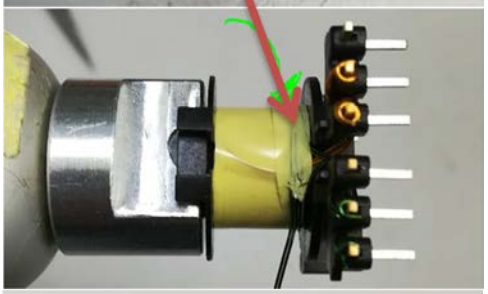
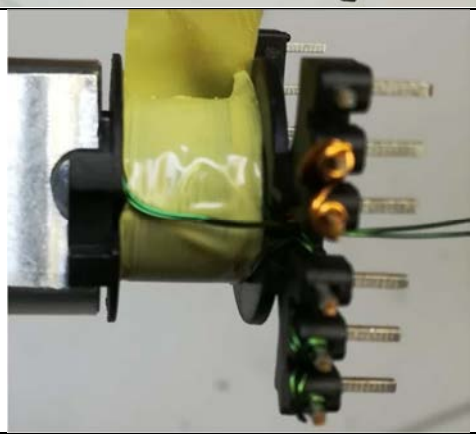
10.7 ***Construction***

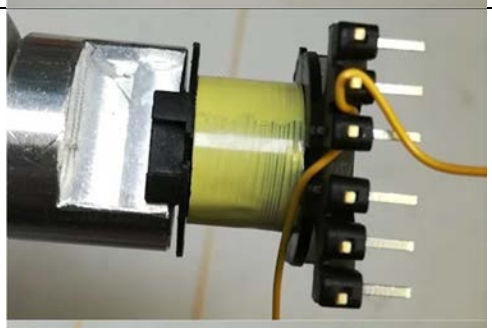
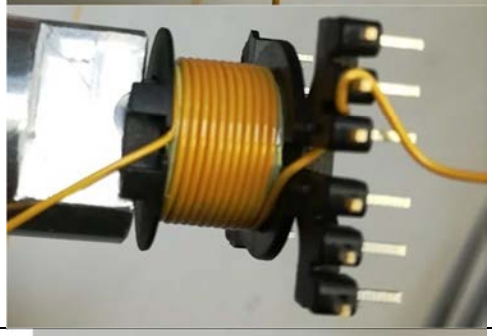
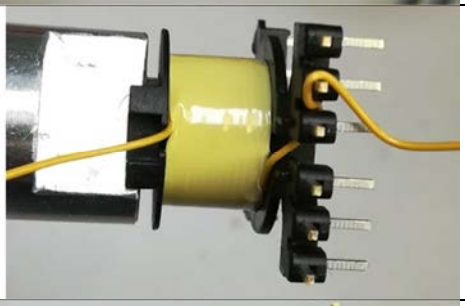
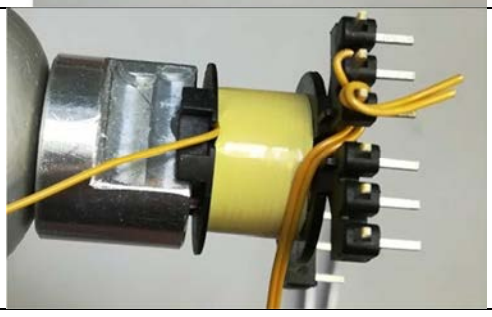
Layer 1 Primary-1	Start at pin 5, wind 16 turns of wire Item [4] in 1 layer with tight tension, at the last turn leave ~2 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [7] for insulation.
Primary-1 termination	Terminate Primary-1 to pin 4 and place another layer of tape.
Layer 2 Primary Bias	Start at pin 1, wind 4 turns of 2 wires Item [3] in 1 layer with tight tension and terminate at pin 2.
Layer 2 Screen: 1	Start at the bobbin (next to Bias wires) with a tape, wind 12 turns of 2 wires Item [3] in 1 layer with tight tension, at the last turn leave ~2 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [7] for insulation.
Screen: 1 Termination	Terminate screen: 1 to pin 3 and place another layer of tape.
Layer 3 LED	Start at pin 11, wind 12 turns of wire Item [5] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [7] for insulation.
Layer 4 CV2	Start at pin 10, wind 5 turns of 2 wires Item [6] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [7] for insulation.
Layer 5 CV1	Start at pin 9, wind 3 turns of 3 wires Item [6] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [7] for insulation.
Layer 6 Screen: 2	Take two wires Item [3], #1 on the start at the bobbin and with a tape and #2 to pin 3, wind 12 turns of the 2 wires in tight tension. At the last turn tape wire #1 to the bobbin and leave ~4 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [7] for insulation.
Screen: 2 Termination	Terminate Screen: 2 screen wire #1 to pin 3 and place another layer of tape.
Layer 7 Primary-2	Start at pin 4, wind 16 turns of wire Item [4] in 1 layer with tight tension, at the last turn leave ~2 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [7] for insulation.
Layer 7 Termination	Terminate Primary-2 screen to pin 6 and place another layer of tape.
Insulation	Place 1 layer of tape Item [7] for insulation.
CV1 termination	Terminate CV1 wires to pin 12.
CV2 termination	Terminate CV2 wires to pin 8.
LED termination	Terminate LED wires to pin 7.
Insulation	Place 1 layer of tape [7] for insulation.
Finish Assembly	Gap core halves to 320 µH inductance (about 0.332 mm air gap). Use clamps [8] and cut only one of the clamps pin (see pic in the next section) Label "DER635SW A3-1 XXX.X µH" (XXX.X primary inductance value in µH) Varnish [9].

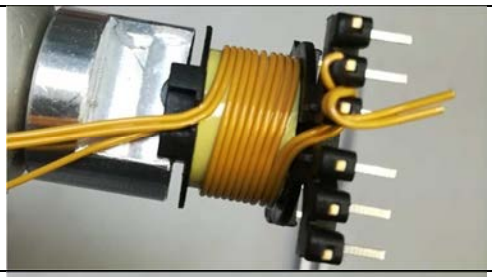
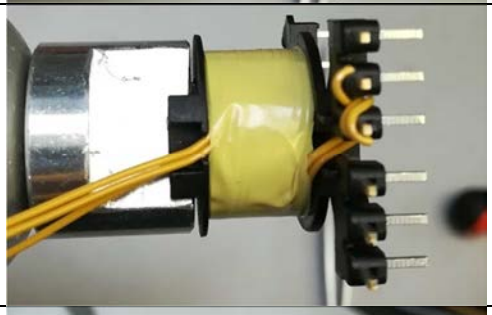
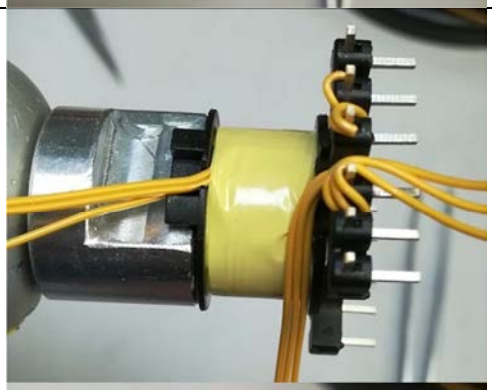
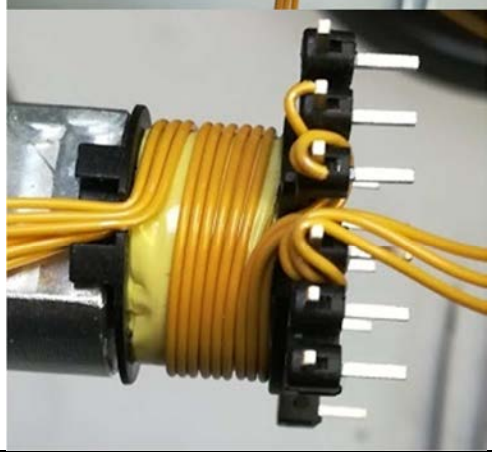
Table 6 – Transformer Winding Instruction.

10.8 *Winding Illustration*

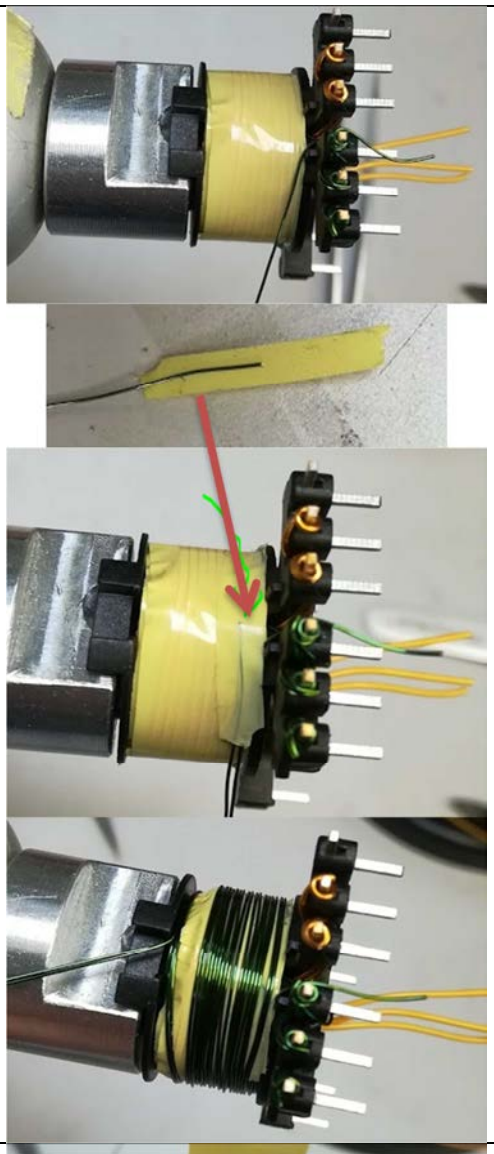
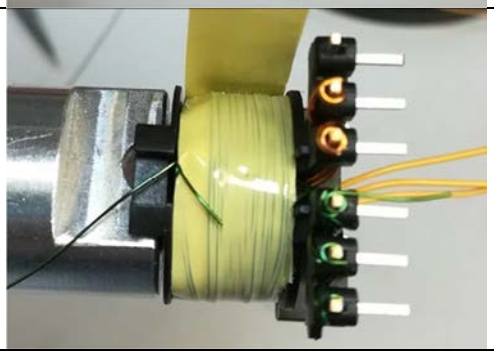
WD1 **½ Primary**		Start at pin 5, wind 16 turns of wire Item [4] in 1 layer with tight tension, at the last turn leave ~2 cm of wire for the termination.
Insulation		Place 1 layer of tape Item [7] for insulation.
WD1 termination		Terminate WD1 primary to pin 4 and place another layer of tape.
WD2 **Bias**		Start at pin 1, wind 4 turns of 2 wires Item [3] in 1 layer with tight tension and terminate at pin 2.

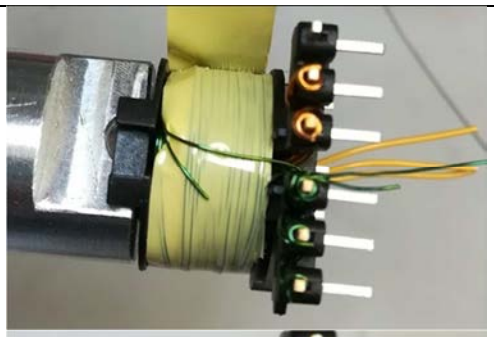
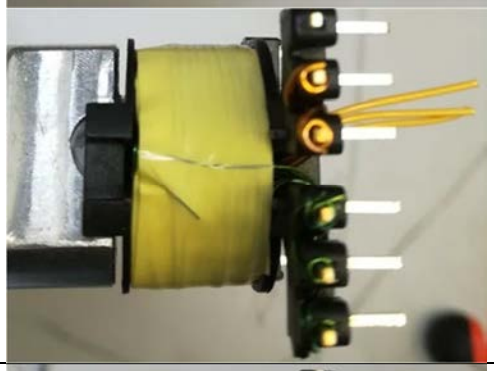
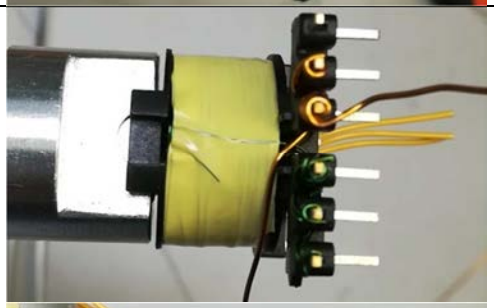
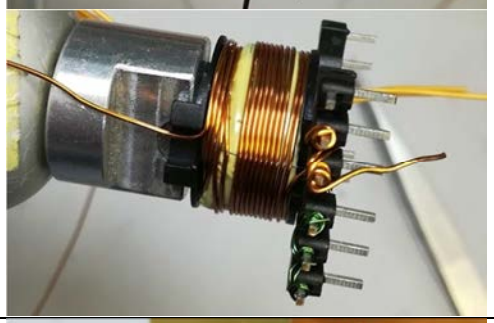
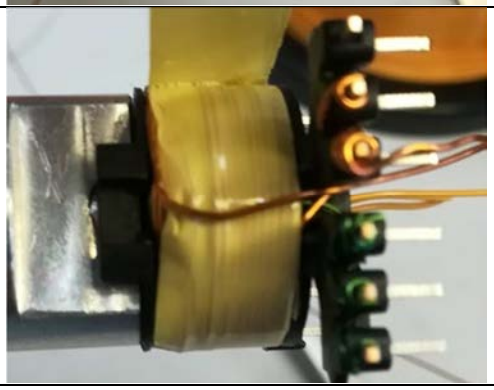
		
WD2 **screen #1**	  	Start at the bobbin (next to Bias wires) with a tape, wind 12 turns of 2 wires Item [3] in 1 layer with tight tension, at the last turn leave ~2 cm of wire for the termination.
Insulation		Place 1 layer of tape Item [7] for insulation.

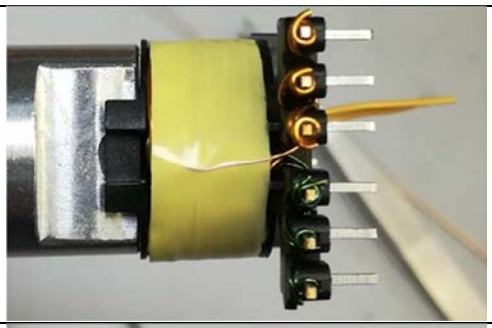
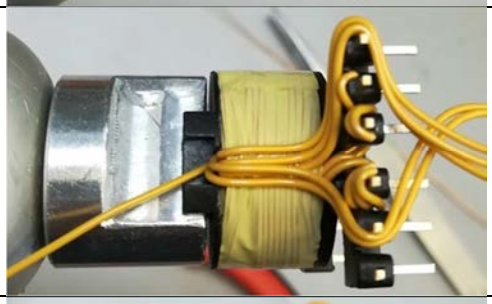
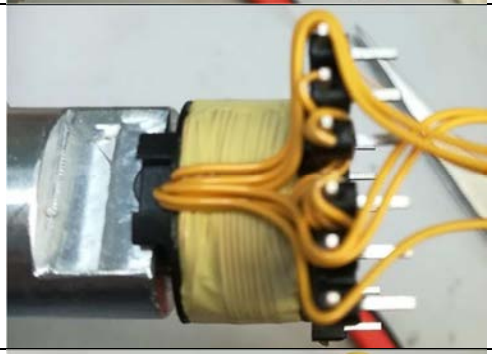
WD2 termination		Terminate WD2 screen to pin 3 and place another layer of tape.
WD3 **LED**	 	Start at pin 11, wind 12 turns of wire Item [5] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.
Insulation		Place 1 layer of tape Item [7] for insulation.
WD4 **CV2**		Start at pin 10, wind 5 turns of 2 wires Item [6] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.

		
Insulation		Place 1 layer of tape Item [7] for insulation.
WD5 **CV1**	 	Start at pin 9, wind 3 turns of 3 wires Item [6] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.

Insulation		Place 1 layer of tape Item [7] for insulation.

WD6 **screen #2**		Take two wires Item [3], #1 on the start at the bobbin and with a tape and #2 to pin 3, wind 12 turns of the 2 wires in tight tension. At the last turn tape wire #1 to the bobbin and leave ~4 cm of wire for the termination.
Insulation		Place 1 layer of tape Item [7] for insulation.

WD6 termination	 	Terminate WD6 screen wire #1 to pin 3 and place another layer of tape.
WD7 **½ Primary**	 	Start at pin 4, wind 16 turns of wire Item [4] in 1 layer with tight tension, at the last turn leave ~2 cm of wire for the termination.
Insulation		Place 1 layer of tape Item [7] for insulation.

WD7 termination		Terminate WD2 screen to pin 6 and place another layer of tape.
WD5 termination		Terminate WD5 wires to pin 12.
WD4 termination		Terminate WD4 wires to pin 8.
WD3 termination		Terminate WD5 wires to pin 7.
Insulation		Place 1 layer of tape Item [7] for insulation.

Finish Assembly		Gap core halves to 320 µH inductance, put clamps Item [8] and cut one of the pins and varnish Item [9].

Table 7 – Transformer Winding Illustration.

10.9 ***Test***

Test the inductance of all the windings

	[µH]	Pins
$L_{pri-lkg}$*	4.46	5-6
L_{pri}	320	5-6
L_{CV1}	2.8	9-12
L_{CV2}	7.8	8-10
L_{LED}	44.8	7-11
$L1_{Saux}$	5	1-2

Table 8 – Transformer Inductance Measurment.

*short all other pins but 5-6.
All measurement done in 100 kHz at 1 V_{RMS}.

11 Performance Data

11.1 *Full Load Efficiency vs. Line*

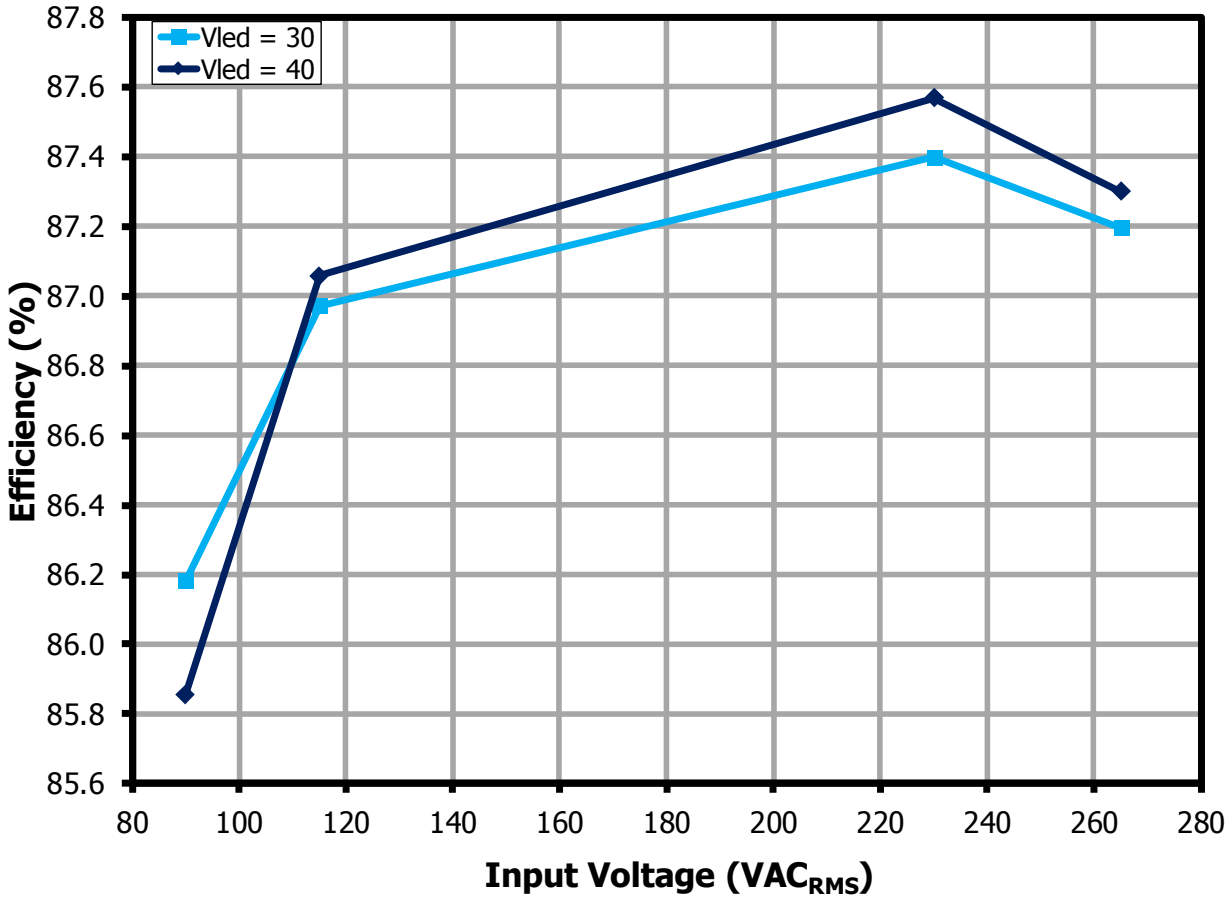


Figure 19 – Full Load Efficiency vs. Line Voltage, Room Temperature.

11.2 *Efficiency vs. Load for all Lines*

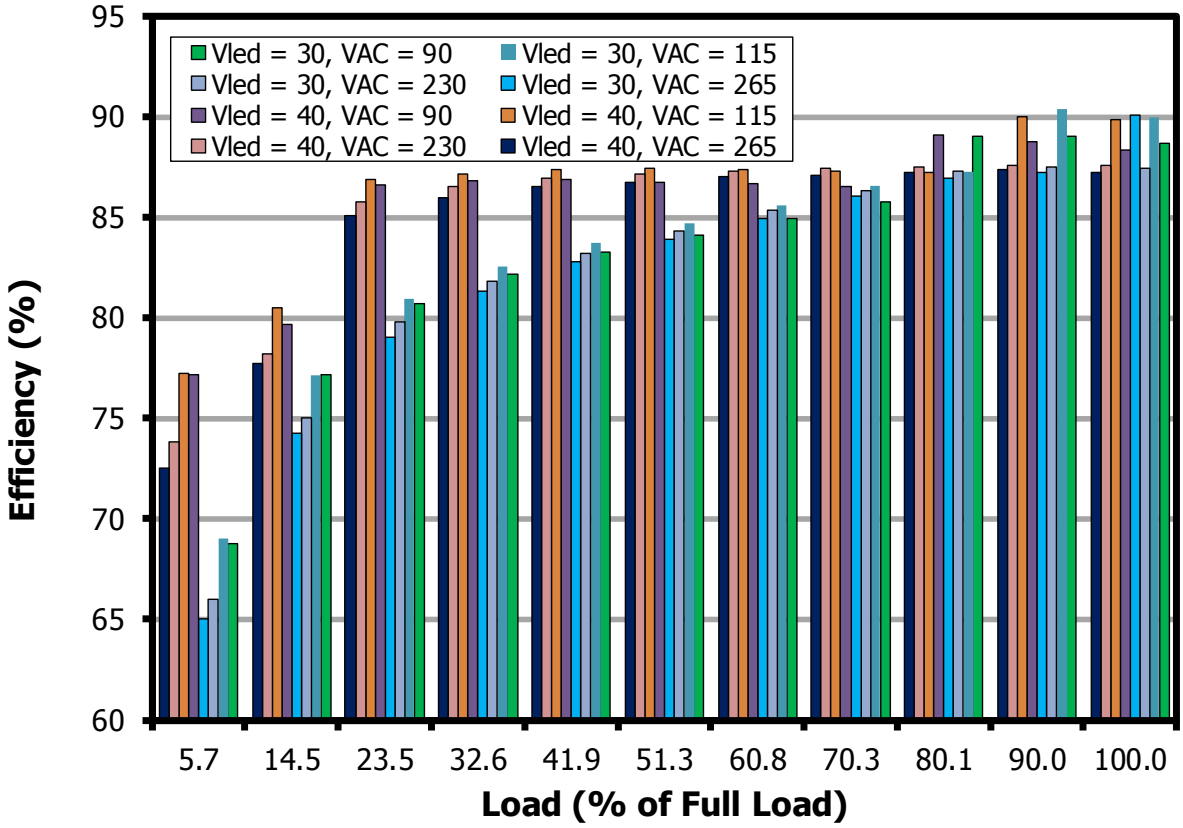


Figure 20 – Efficiency vs. Load, Room Temperature.

11.3 *Line Regulation at Full Load*

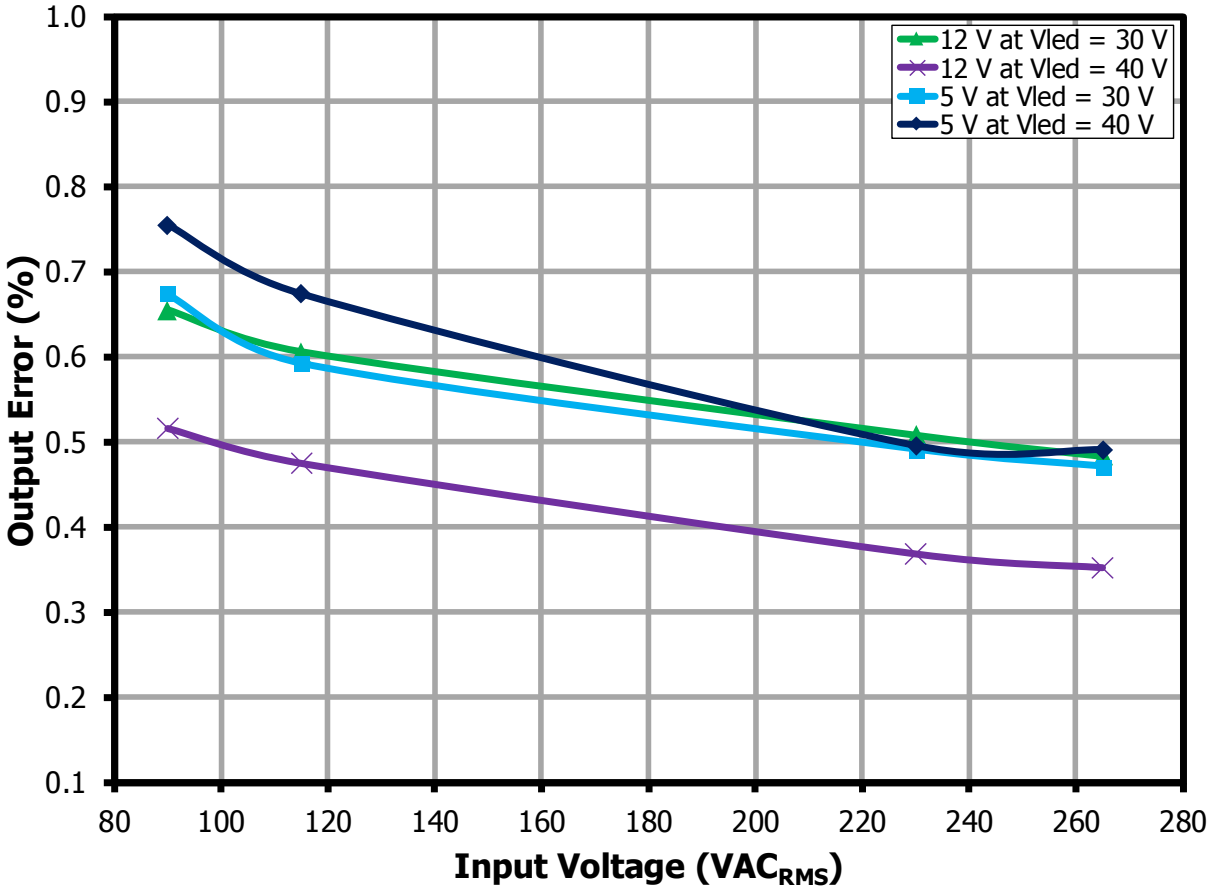


Figure 21 – Output Voltage vs. Line, Room Temperature.

11.4 *5 V Output Load Regulation*

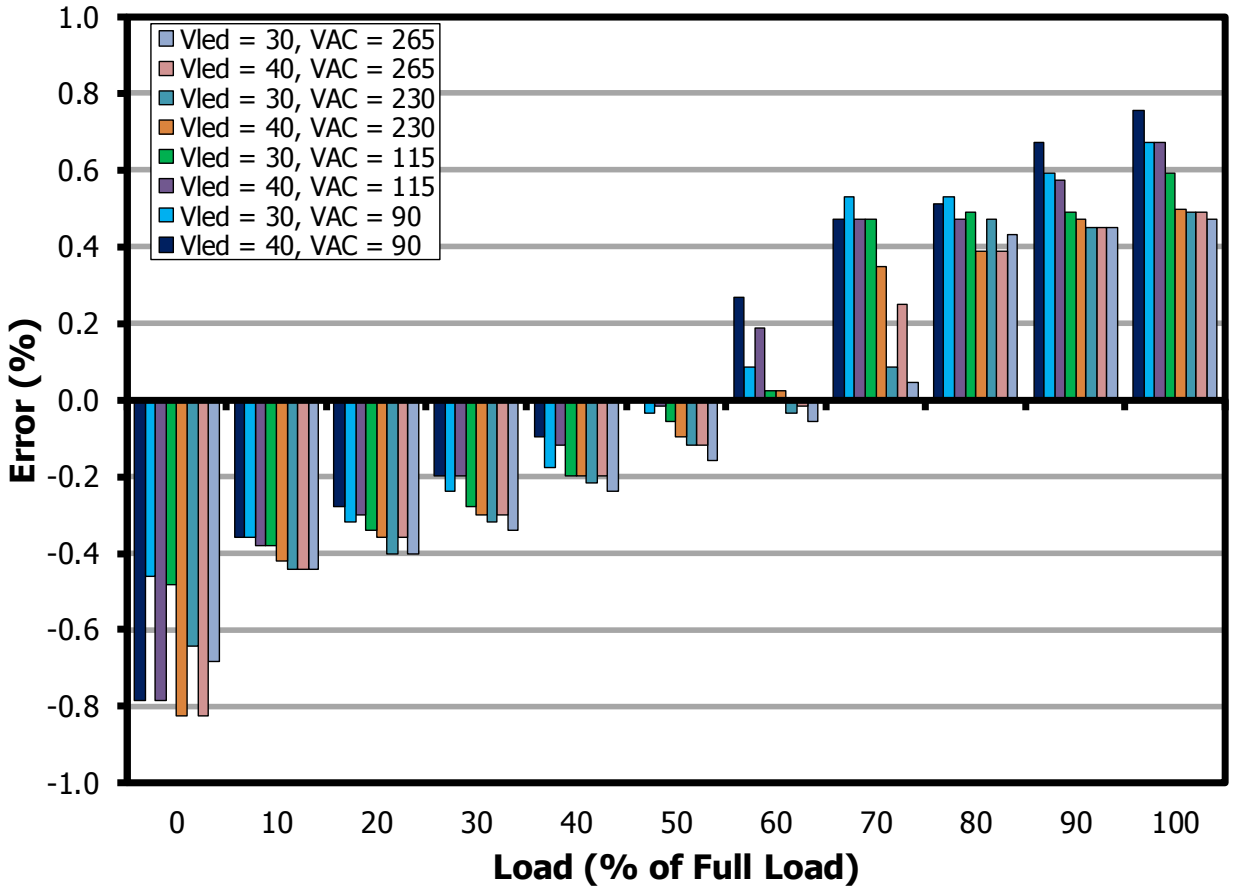


Figure 22 – 5 V Output vs. 5 V Load, Room Temperature.

11.5 *12 V Output Load Regulation*

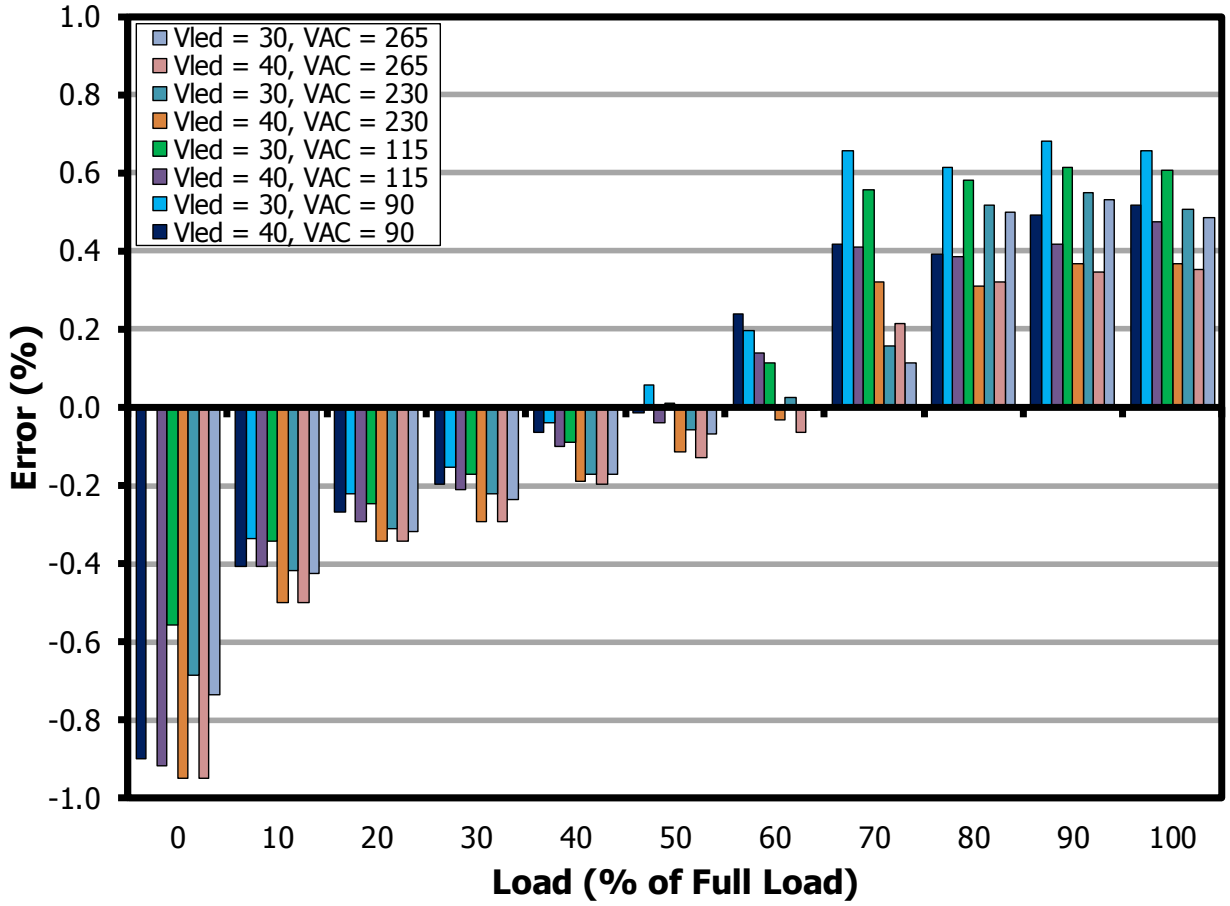


Figure 23 – 12 V Output vs. 12 V Load, Room Temperature.

11.6 *Input Power with Minimum Load (5 V @ 0 A, 12 V @ 0 A, 40 V @ 0 A)*

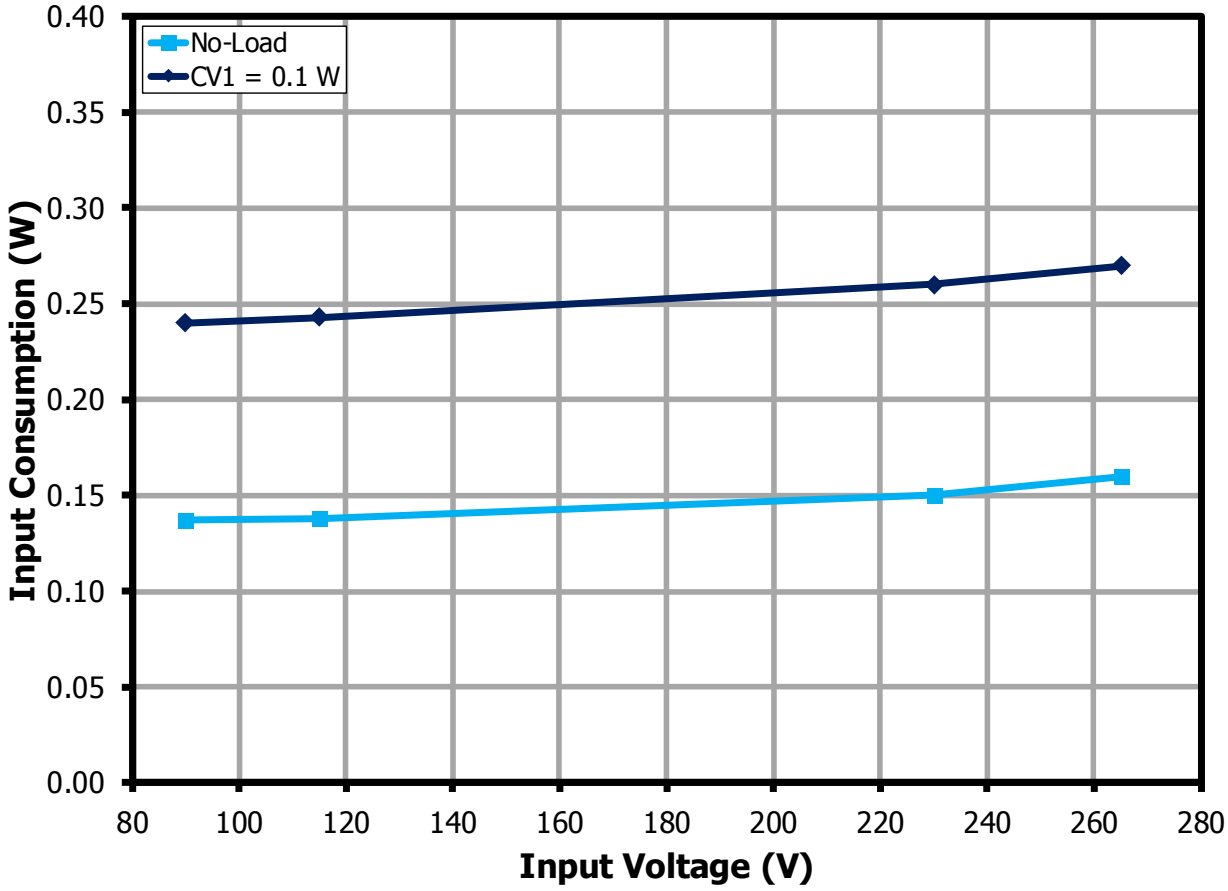


Figure 24 – Input Power vs. Input Voltage, Room Temperature.

11.7 *LED Dimming*

11.7.1 Analog Dimming

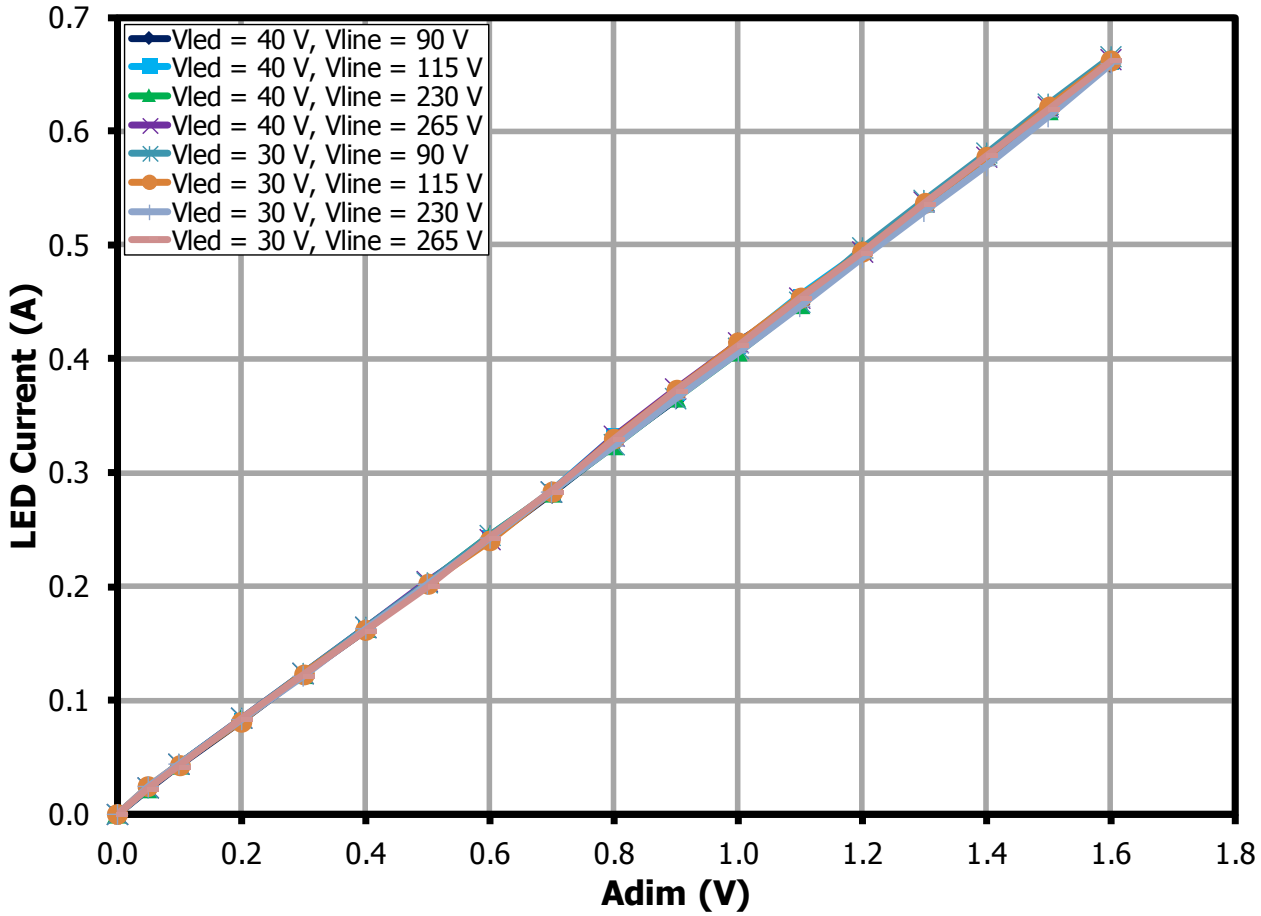


Figure 25 – Analog Dimming.

11.7.2 PWM Dimming

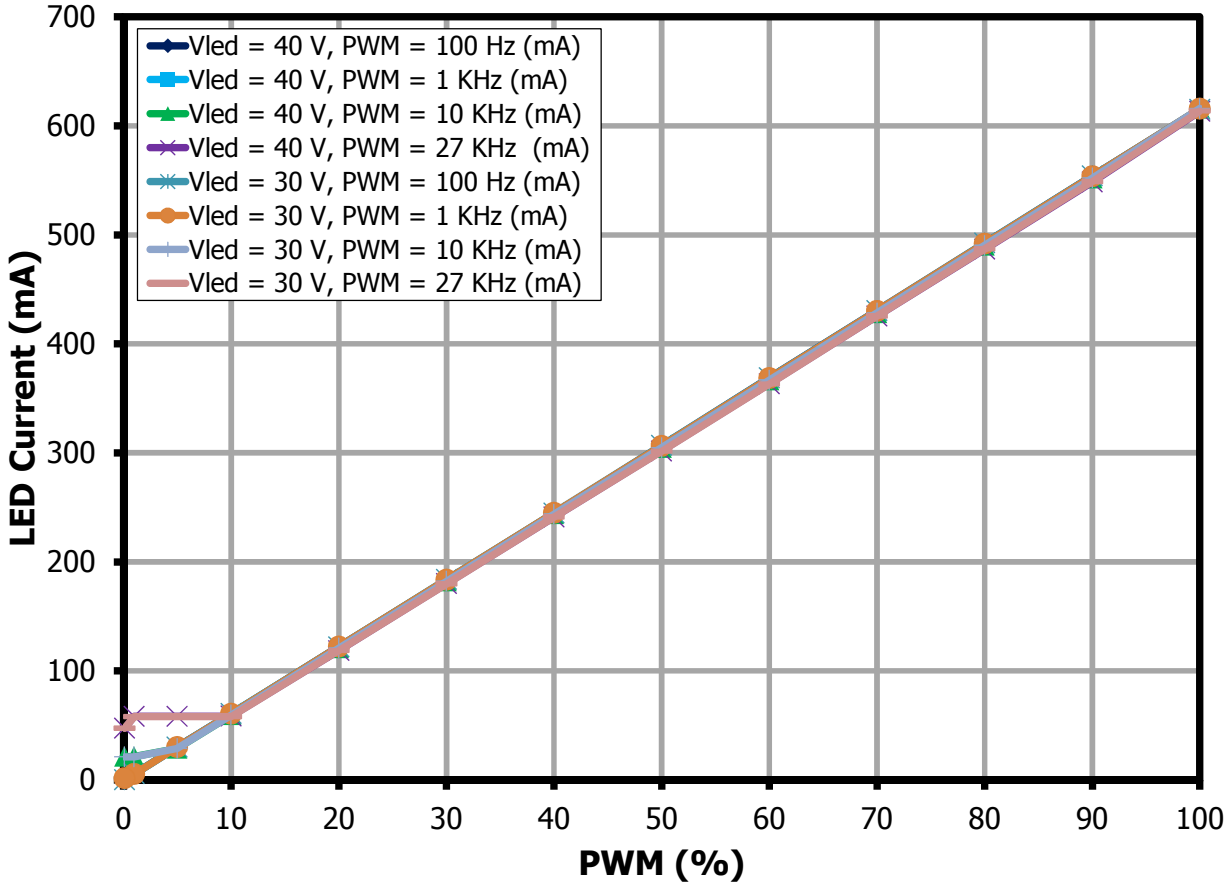


Figure 26 – PWM Dimming.

Low frequency

Channel 2	Channel 6	Channel 4	Channel 5
Iled total [200mA/div]	PWM [5V/div]	Vled+ [20V/div]	Vled RTN [20V/div]

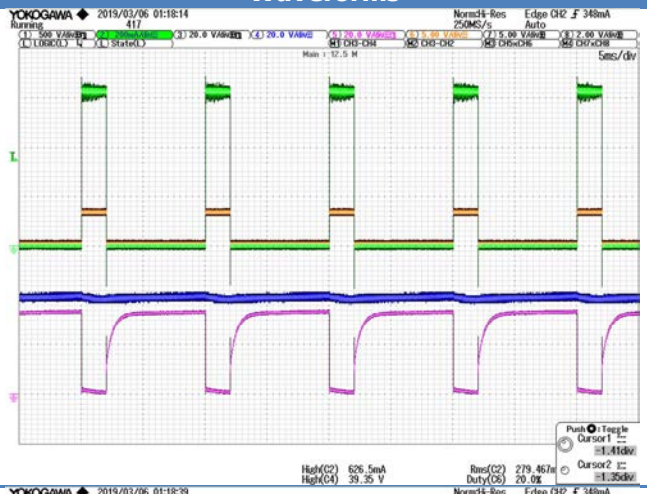
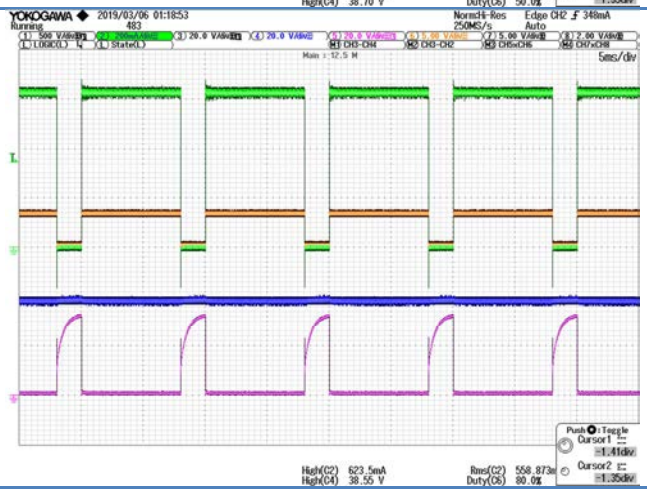
Working point	Waveforms
100Hz **20% Duty cycle** **I_LED Is 280mA**	
100Hz **50% Duty cycle** **I_LED Is 440mA**	
100Hz **80% Duty cycle** **I_LED Is 560mA**	

Figure 27 – Low Frequency PWM Waveform.

Medium frequency

Channel 2	Channel 6	Channel 4	Channel 5
Iled total [200mA/div]	PWM [5V/div]	Vled+ [20V/div]	Vled RTN [20V/div]

Working point	Waveforms
10KHz **20% Duty cycle** **I_LED Is 280mA**	
3KHz **50% Duty cycle** **I_LED Is 440mA**	
3KHz **80% Duty cycle** **I_LED Is 555mA**	

Figure 28 – Meduim Frequency PWM Waveform.

High frequency

Channel 2	Channel 6	Channel 4	Channel 5
Iled total [200mA/div]	PWM [5V/div]	Vled+ [20V/div]	Vled RTN [20V/div]

Working point	Waveforms
27KHz **20% Duty cycle** **I_LED Is 260mA**	
27KHz **50% Duty cycle** **I_LED Is 425mA**	
27KHz **80% Duty cycle** **I_LED Is 555mA**	

Figure 29 – High Frequency PWM Waveform.

12 Waveforms

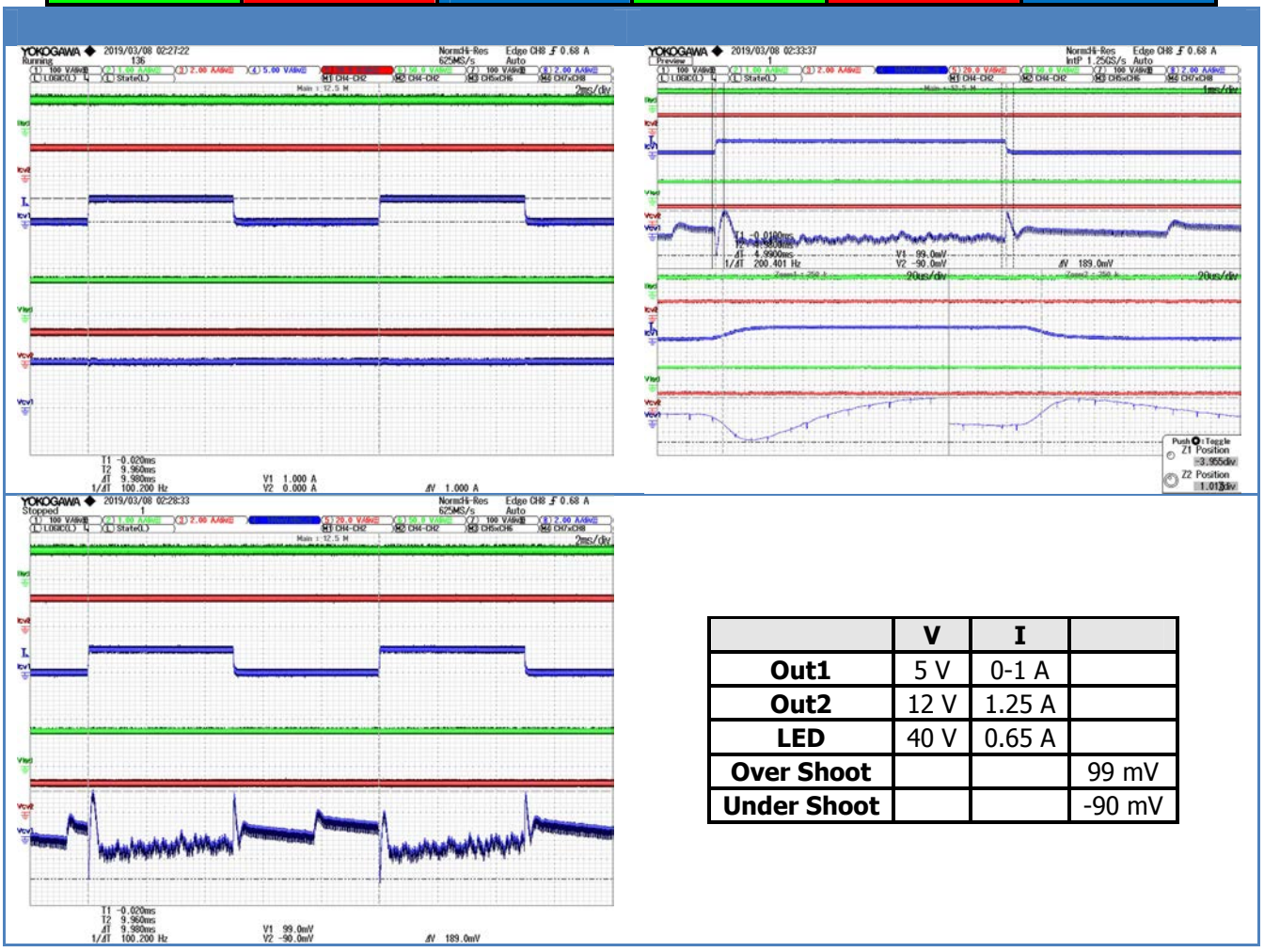
12.1 *Load Transient Response*

12.1.1 5 V Load transient

Test was performed at 230 VAC, CV1 load set to 1 A, CV2 load set to 1.25 A and 40 V LED panel used.

0 A – 1 A – 0 mA transient load applied to CV1 output at a 100 Hz rate, 50% duty cycle.

Channel 2	Channel 5	Channel 8	Channel 6	Channel 3	Channel 4
I led	I cv2	I cv1	V led	V cv2	V cv1



	V	I	
Out1	5 V	0-1 A	
Out2	12 V	1.25 A	
LED	40 V	0.65 A	
Over Shoot			99 mV
Under Shoot			-90 mV

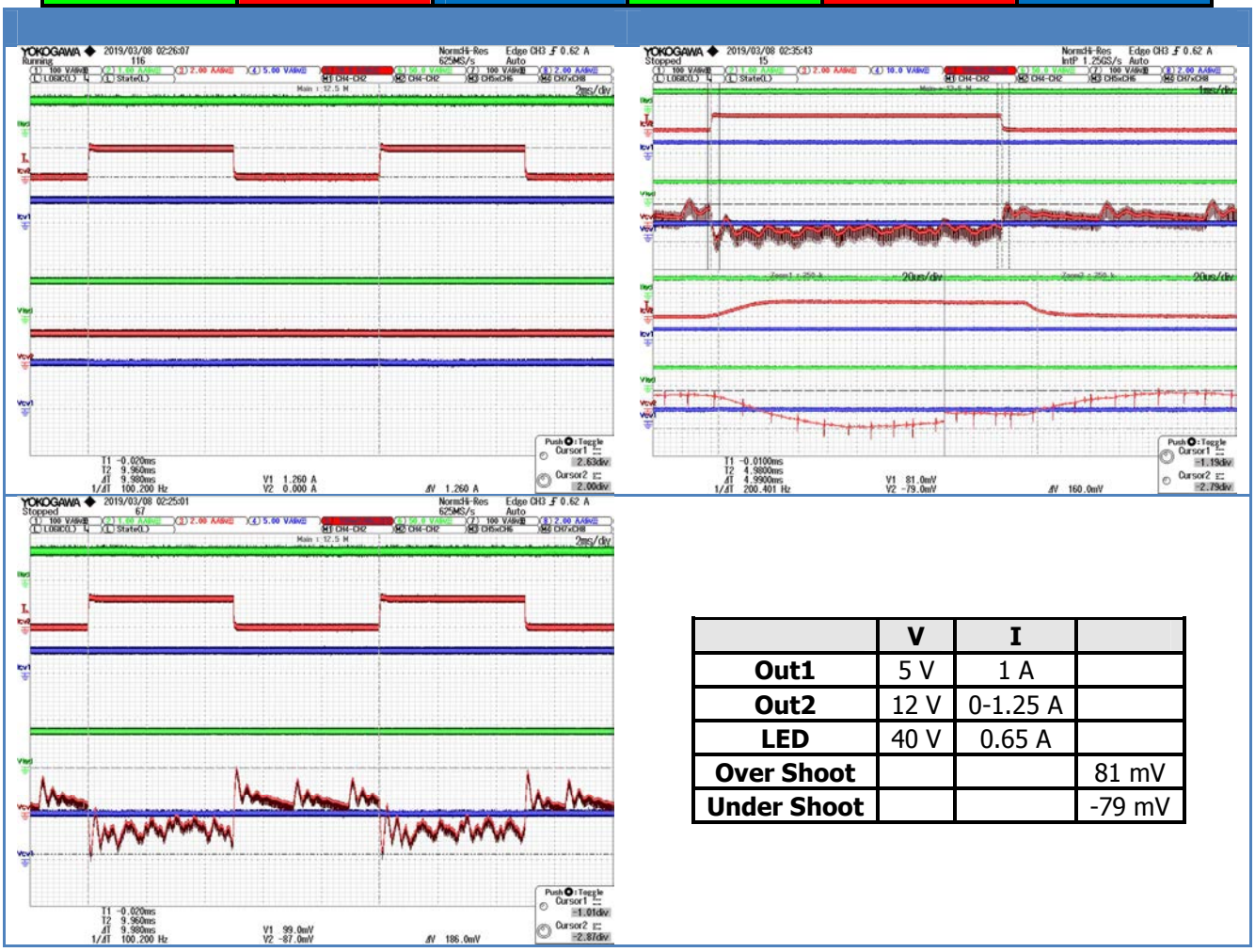
Figure 30 – CV1 (5 V) Output - Load Transient.

12.1.2 12 V Load Transient

Test was performed at 230 VAC, CV1 load set to 1 A, CV2 load set to 1.25 A and 40 V LED panel used.

0 A – 1.25 A – 0 mA transient load applied to CV2 output at a 100 Hz rate, 50% duty cycle.

Channel 2	Channel 5	Channel 8	Channel 6	Channel 3	Channel 4
I led	I cv2	I cv1	V led	V cv2	V cv1



	V	I	
Out1	5 V	1 A	
Out2	12 V	0-1.25 A	
LED	40 V	0.65 A	
Over Shoot			81 mV
Under Shoot			-79 mV

Figure 31 – CV2 (12 V) Output - Load Transient.

12.2 *Switching Waveforms*

12.2.1 Maximum Voltage on the Primary Transistor

Voltages on the primary transistor drain to source on each pulse (LED, Vo2 and Vo1). Test condition is full load and maximum voltage, 375 VDC (equal to the peak of 265 VAC).

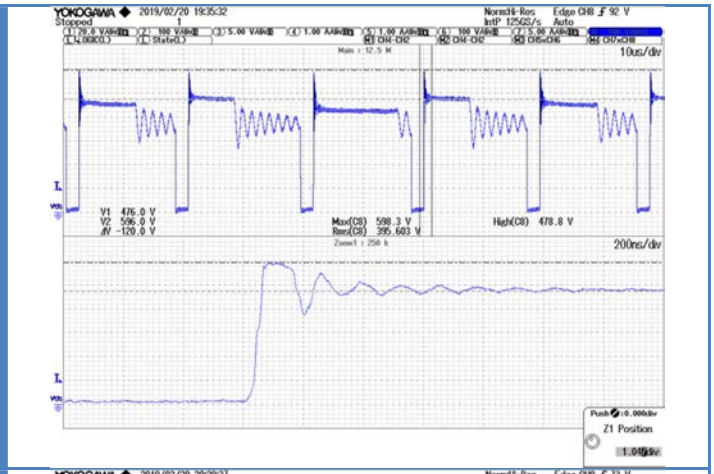
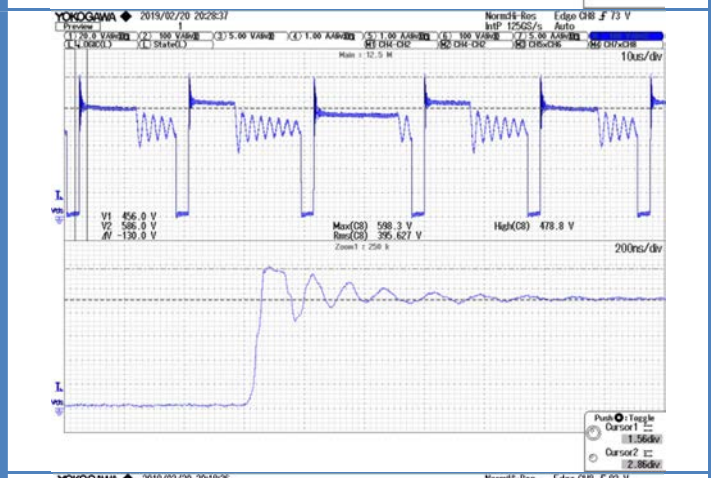
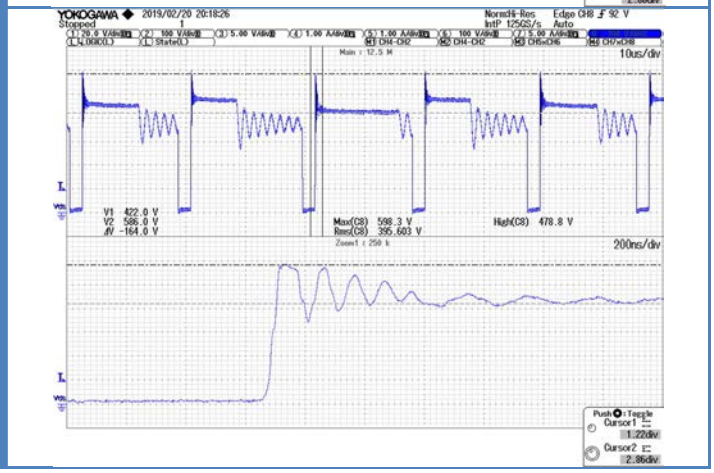
LED pulse **Peak voltage measured 596V** **High voltage measured 476V** **Reflected voltage measured 476V-375V=101V** **Reflected voltage Calculated 40V*32/12=107V**	
Vo2 pulse **Peak voltage measured 586V** **High voltage measured 456V** **Reflected voltage measured 456V-375V=81V** **Reflected voltage Calculated 12V*32/12=77V**	
Vo1 pulse **Peak voltage measured 586V** **High voltage measured 422V** **Reflected voltage measured 422V-375V=47V** **Reflected voltage Calculated 5V*32/3=53V**	

Figure 32 – Maximum Voltage Vds Waveform.

12.2.2 Primary Frequency

Average and maximum frequency at 90 VAC at full load.

LED pulse **Maximum frequency (at lowest voltage)** **86.56KHz**	 Vds Pri –yellow Vgs SR - purple
Average frequency (at full cycle) **82.46KHz**	 Vds Pri –yellow Vgs SR - purple

Figure 33 – Maximum Frequency Waveform.

12.2.3 Currents Waveform

Average and maximum currents (Peak, RMS and average) at 90 VAC @ full load.

LED pulse

Maximum currents (at lowest voltage)

	rms [A]	Pk [A]	Avg [A]
Pri	0.83	2.14	0.5
SR	5.17	20.8	2.79
Io1	3.83	21.4	1.02
Io2	3.02	13.4	1.13
Iled	1.34	8.8	0.49

Average currents (at full cycle)

	rms [A]	Pk [A]	Avg [A]
Pri	0.81	2.2	0.46
SR	5.26	21.8	2.91
Io1	3.83	22.4	0.99
Io2	3.13	14	1.2
Iled	1.47	9.1	0.58

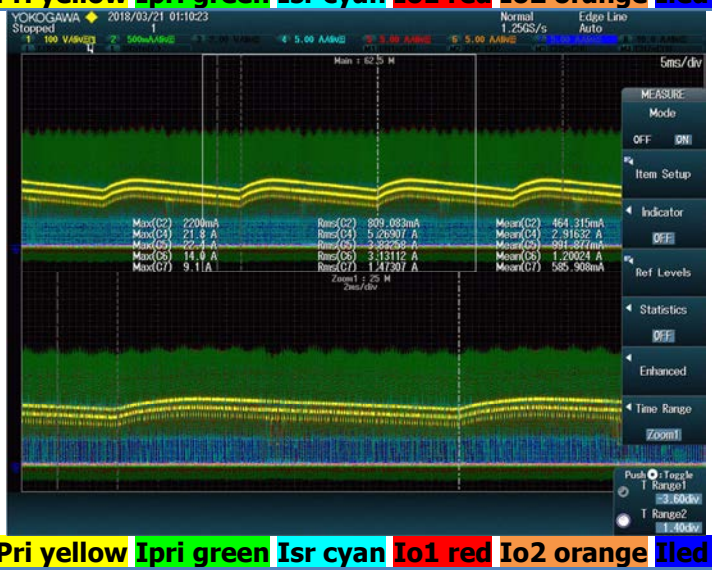
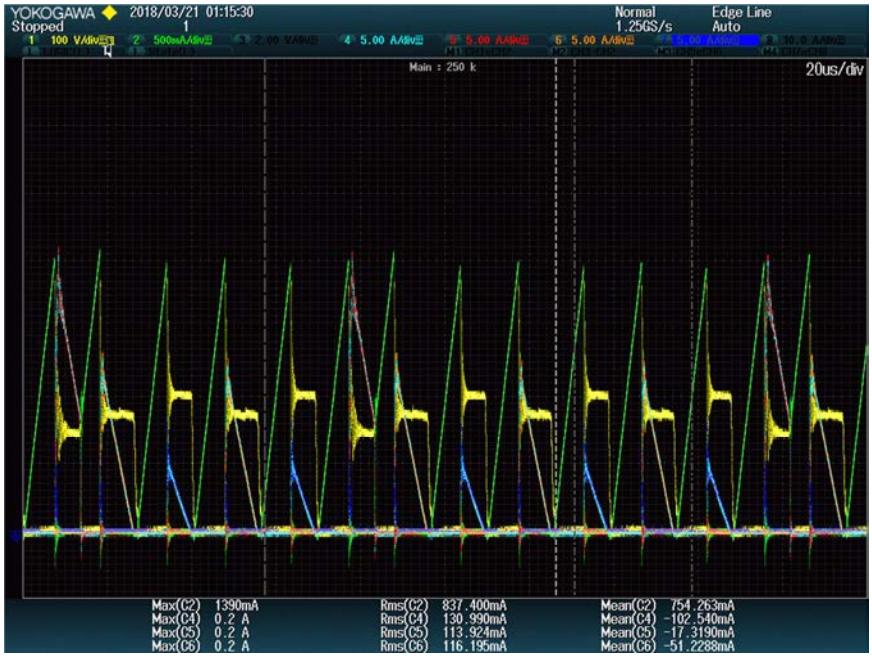


Figure 34 – Currents Waveform.



Vds Pri yellow **Ipri green** **Isr cyan** **Io1 red** **Io2 orange** **Iled blue**

Figure 35 – Zoom on Transformer Pri/Sec Current Waveform.

Isr cyan **Io1 red** **Io2 orange** **Iled blue**

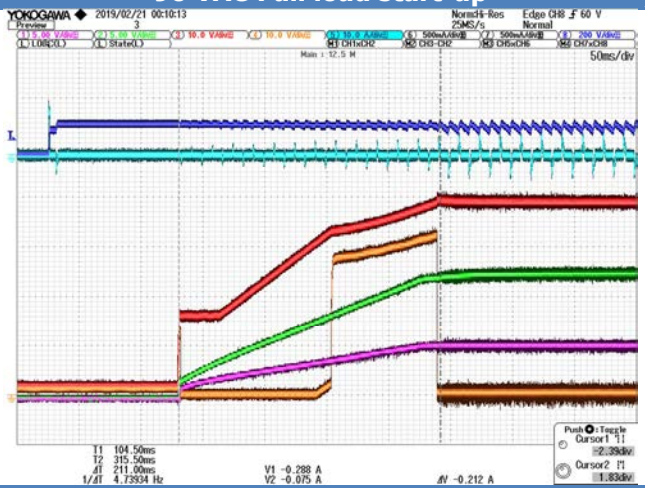
Figure 36 – Zoom on Transformer Sec Current Waveform.

12.3 *Start-Up Waveform*

12.3.1 Starting-up with Full Load

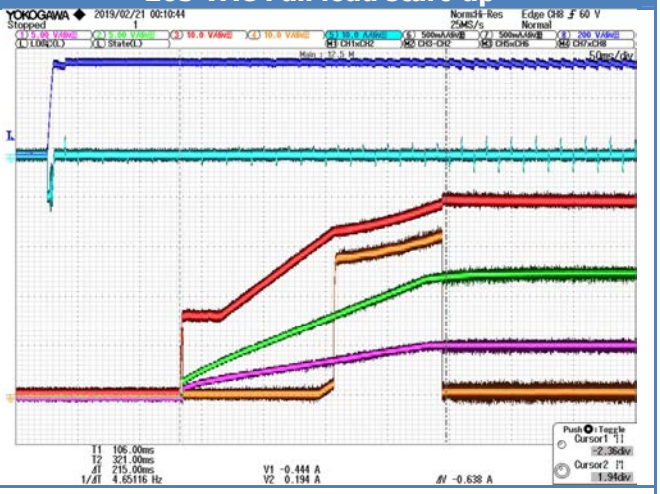
Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 8
Vo1 [10V/div]	Vo2 [10V/div]	LED [10V/div]	RTN [10V/div]	Iac [10A/div]	Vds [200V/div]

90 VAC Full load start-up



	V	I
Input	90 VAC	
Out1	5 V	1 A
Out2	12 V	1.25 A
LED	40 V	0.65 A
Start-up time	104 ms	
Stable time	211 ms	

265 VAC Full load start-up



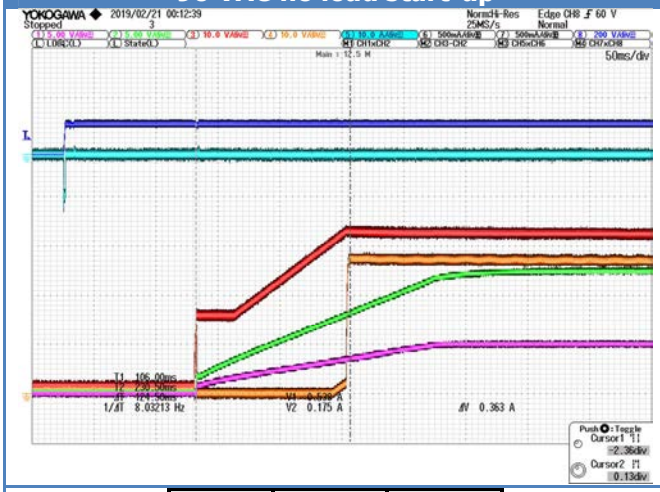
	V	I
Input	265 VAC	
Out1	5 V	1 A
Out2	12 V	1.25 A
LED	40 V	0.65 A
Start-up time	106 ms	
Stable time	215 ms	

Figure 37 – Start-up Waveform with Full Load.

12.3.2 Starting-up with No-Load

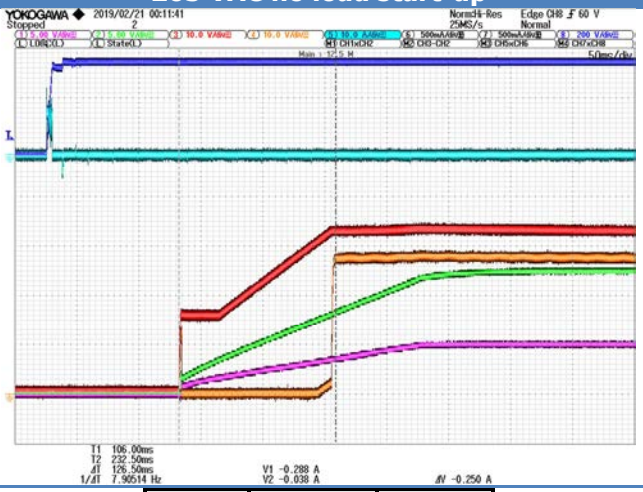
Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 8
Vo1 [10V/div]	Vo2 [10V/div]	LED [10V/div]	RTN [10V/div]	Iac [10A/div]	Vds [200V/div]

90 VAC no load start-up



	V	I
Input	90 VAC	
Out1	5 V	0A
Out2	12 V	0A
LED	0 V	0A
Start-up time		106 ms
Stable time		124 ms

265 VAC no load start-up



	V	I
Input	265 VAC	
Out1	5 V	0 A
Out2	12 V	0 A
LED	0 V	0 A
Start-up time		106ms
Stable time		126 ms

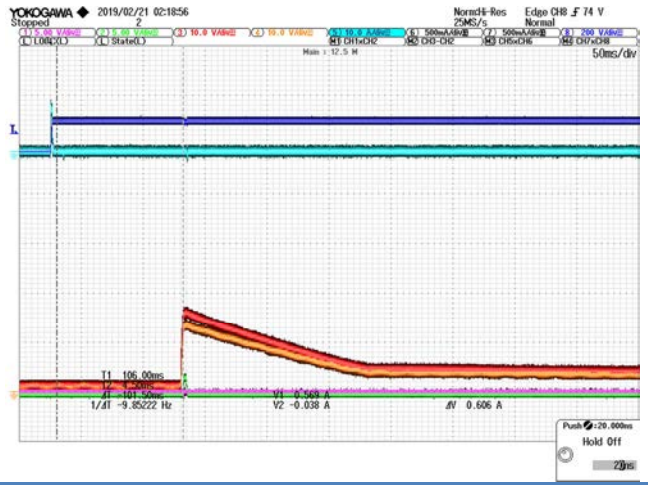
Figure 38 – Start-up Waveform No-Load.

12.3.3 Starting-up with Shorted/No FB 5 V Output

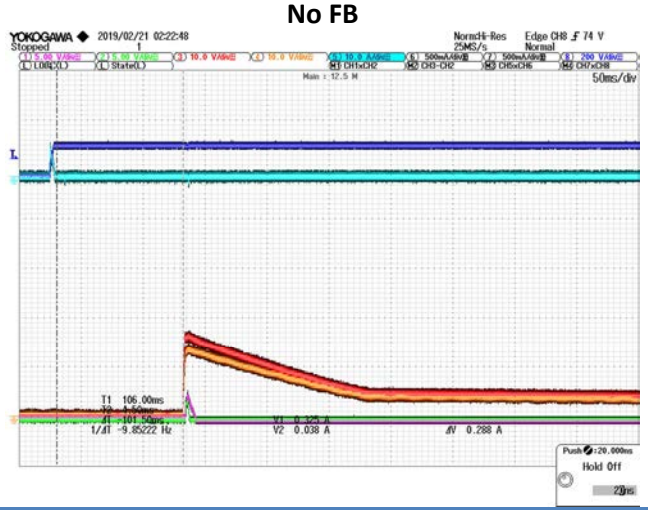
Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 8
Vo1 [10V/div]	Vo2 [10V/div]	LED [10V/div]	RTN [10V/div]	Iac [10A/div]	Vds [200V/div]

90 VAC 5 V shorted/no FB

Short



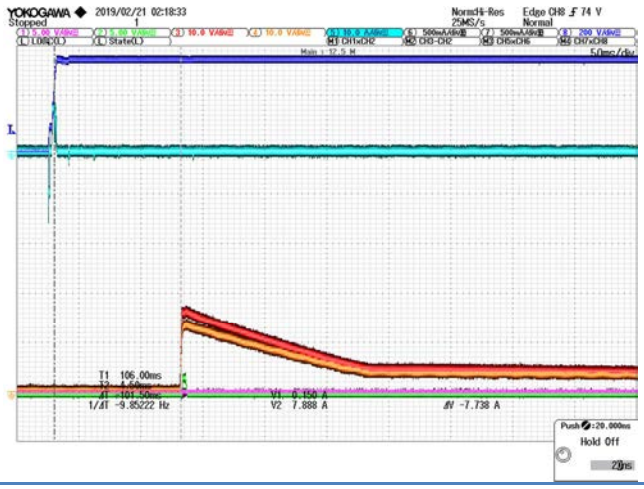
No FB



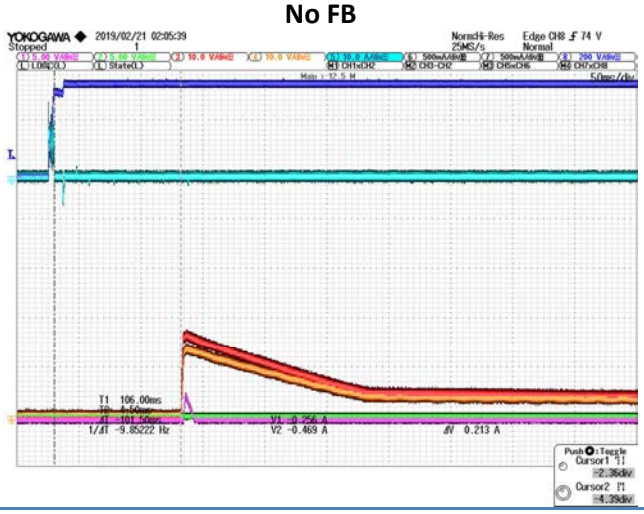
	V	I
Input	90 VAC	
Out1	5 V	Short / no FB
Out2	12 V	1.25 A
LED	40 V	0.65 A
Remark		

265 VAC 5 V shorted/no FB

Short



No FB



	V	I
Input	265 VAC	
Out1	5 V	Short / no FB
Out2	12 V	1.25 A
LED	40 V	0.65 A
Remark		

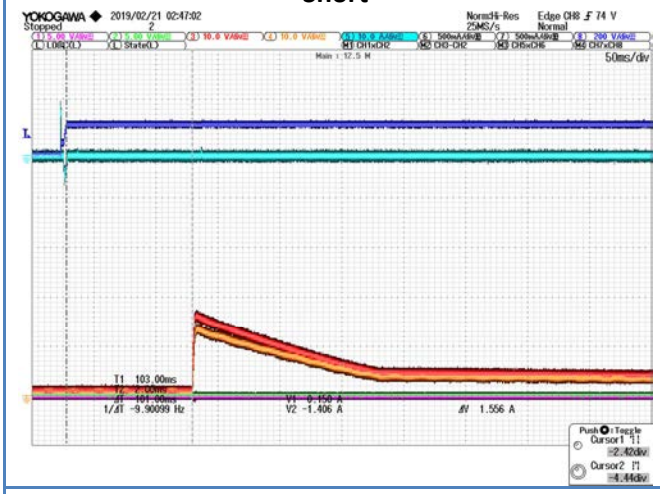
Figure 39 – Starting-up with Shorted CV1 or no FB1.

12.3.4 Starting-up with Shorted/No FB 12V Output

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 8
Vo1 [10V/div]	Vo2 [10V/div]	LED [10V/div]	RTN [10V/div]	Iac [10A/div]	Vds [200V/div]

90 VAC 12 V shorted/no FB

Short

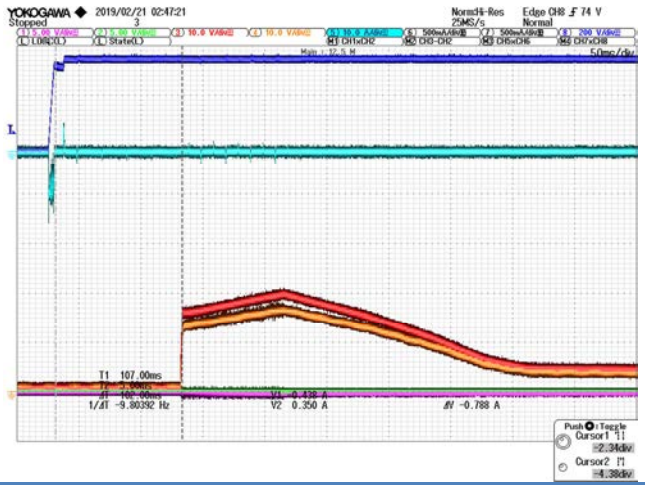


No FB

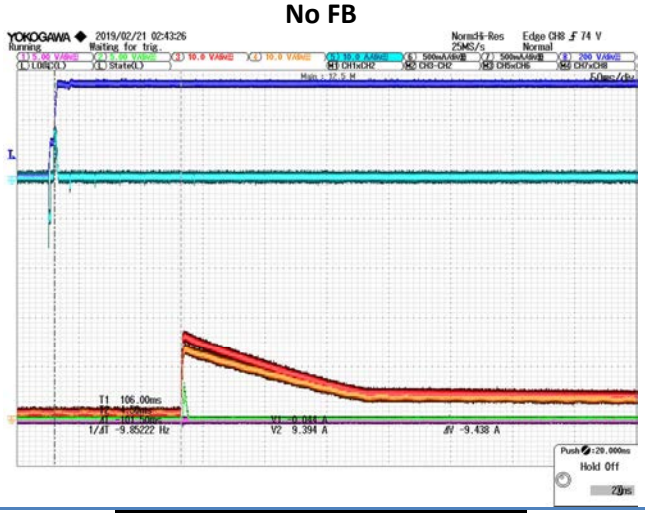
	V	I
Input	90 VAC	
Out1	5 V	1 A
Out2	12 V	Short / no FB
LED	40 V	0.65 A
Remark		

265 VAC 12 V shorted/no FB

Short



No FB



	V	I
Input	265 VAC	
Out1	5 V	1 A
Out2	12 V	Short / no FB
LED	40 V	0.65 A
Remark		

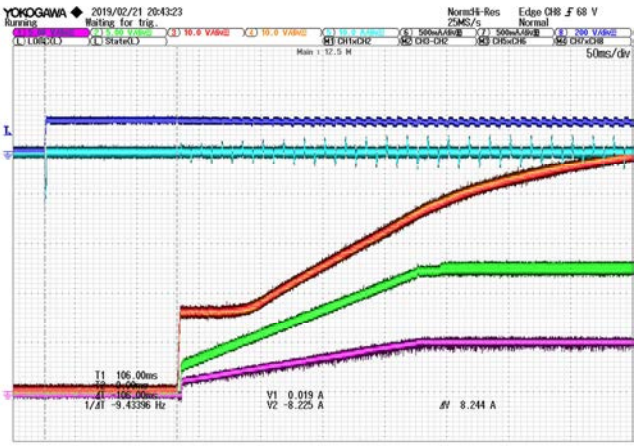
Figure 40 – Starting-up with Shorted CV2 or no FB2.

12.3.5 Starting-up with Shorted/No FB LED Output

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 8
Vo1 [10V/div]	Vo2 [10V/div]	LED [10V/div]	RTN [10V/div]	Iac [10A/div]	Vds [200V/div]

90 VAC LED shorted/no FB

Short

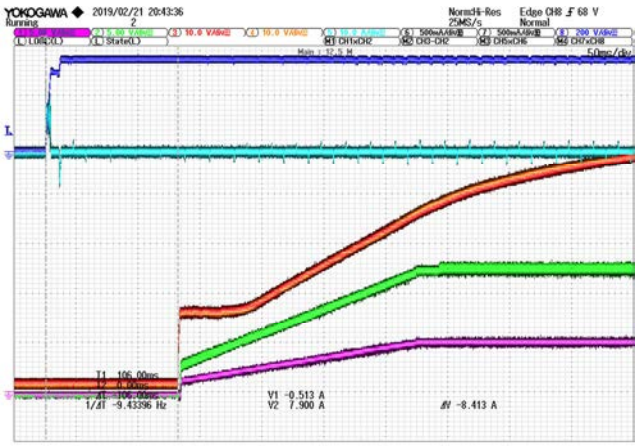


No FB

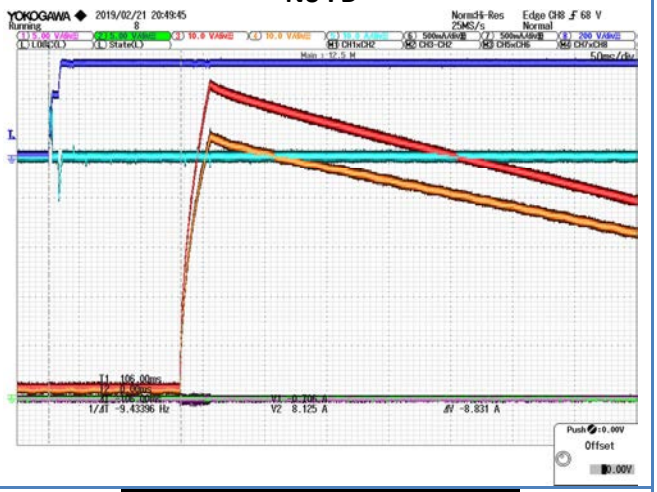
	V	I
Input	90 VAC	
Out1	5 V	1 A
Out2	12 V	1.25 A
LED	40 V	Short/no FB
Remark		

265 VAC LED shorted/no FB

Short



No FB



	V	I
Input	265 VAC	
Out1	5 V	1 A
Out2	12 V	1.25 A
LED	40 V	Short/no FB
Remark		

Figure 41 – Starting-up with Shorted LED output or no FB3.

12.3.6 5 V, 12 V, LED and SR FET/Diode Voltage Waveforms

12.3.6.1 SR Voltage under Full Load at 265 VAC

Channel 5
Vds SR [10V/div]

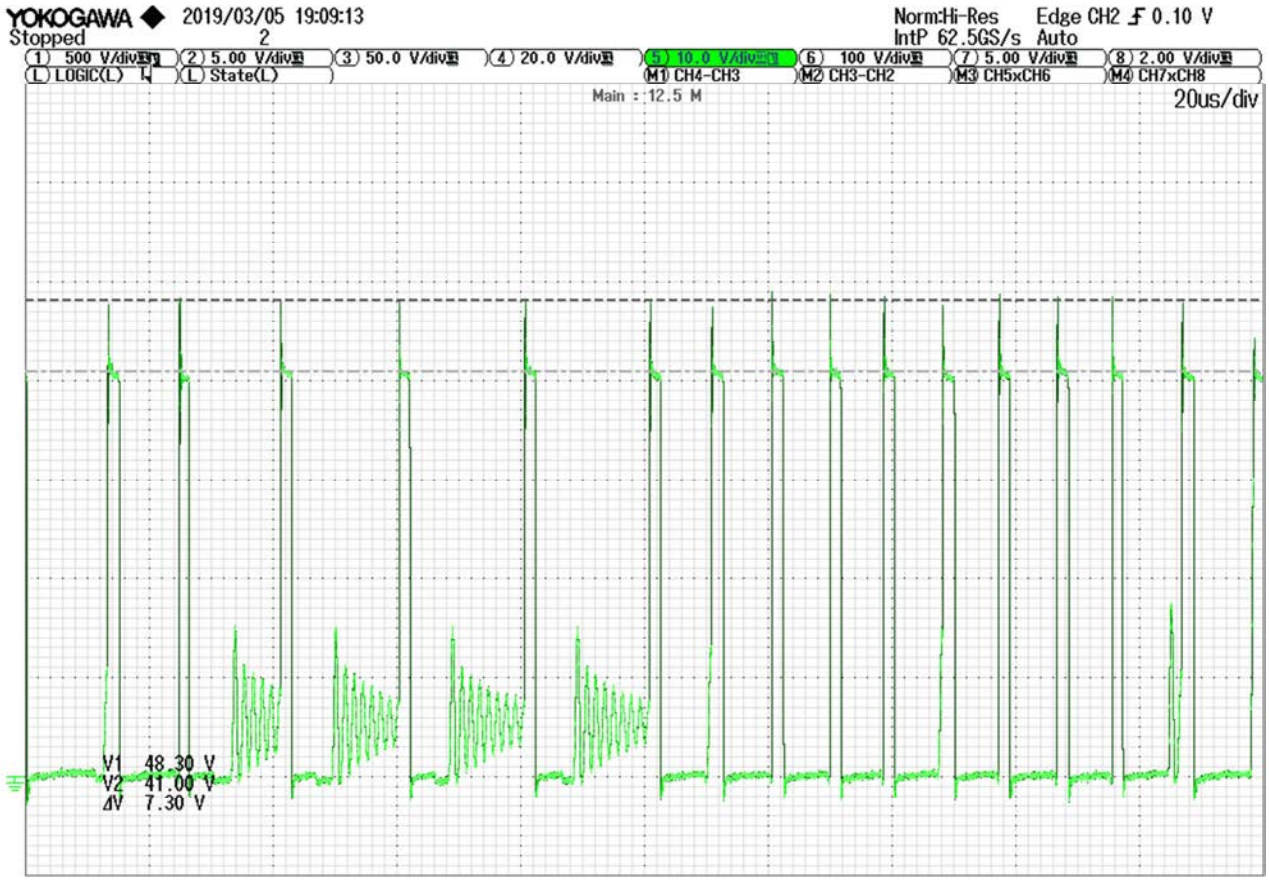


Figure 42 – SR D-S Voltage Under Full Load at 265 VAC.

Maximum voltage on SR is <50 V.

12.3.6.2 Voltage on CV1 Selection FET Under Full Load at 265 VAC

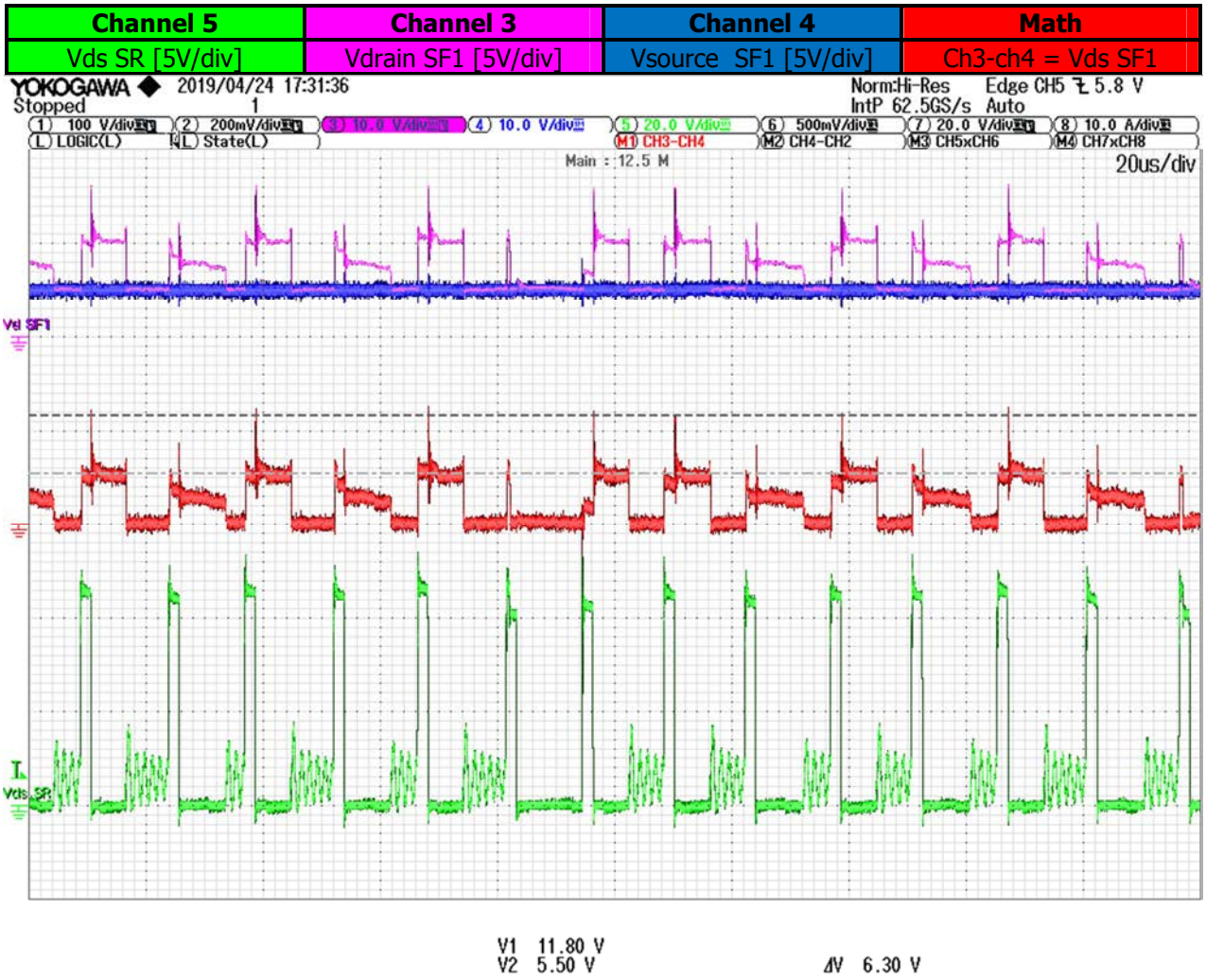


Figure 43 –CV1 Selection FET D-S voltage Under Full Load at 265 VAC.

The maximum D-S voltage across the selection FET of CV1 is <15 V.

12.3.6.3 CV2 Selection FET D-S Voltage Under full load at 265 VAC

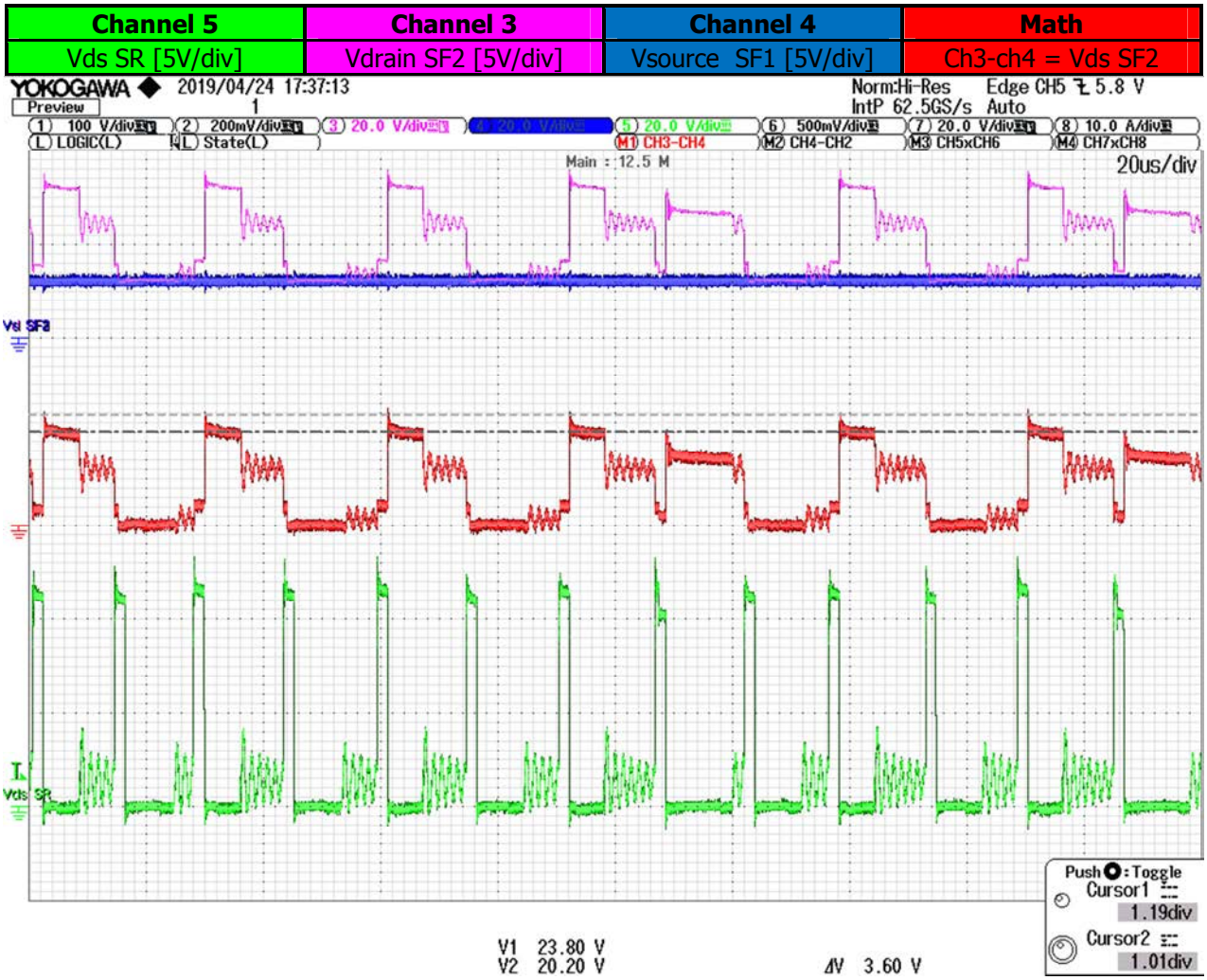


Figure 44 – CV2 selection FET Under full load at 265 VAC line voltage.

The maximum D-S voltage across the CV2 selection FET is <20 V.

12.3.6.4 CV2 Blocking Diode Reverse Voltage under Full Load at 265 VAC

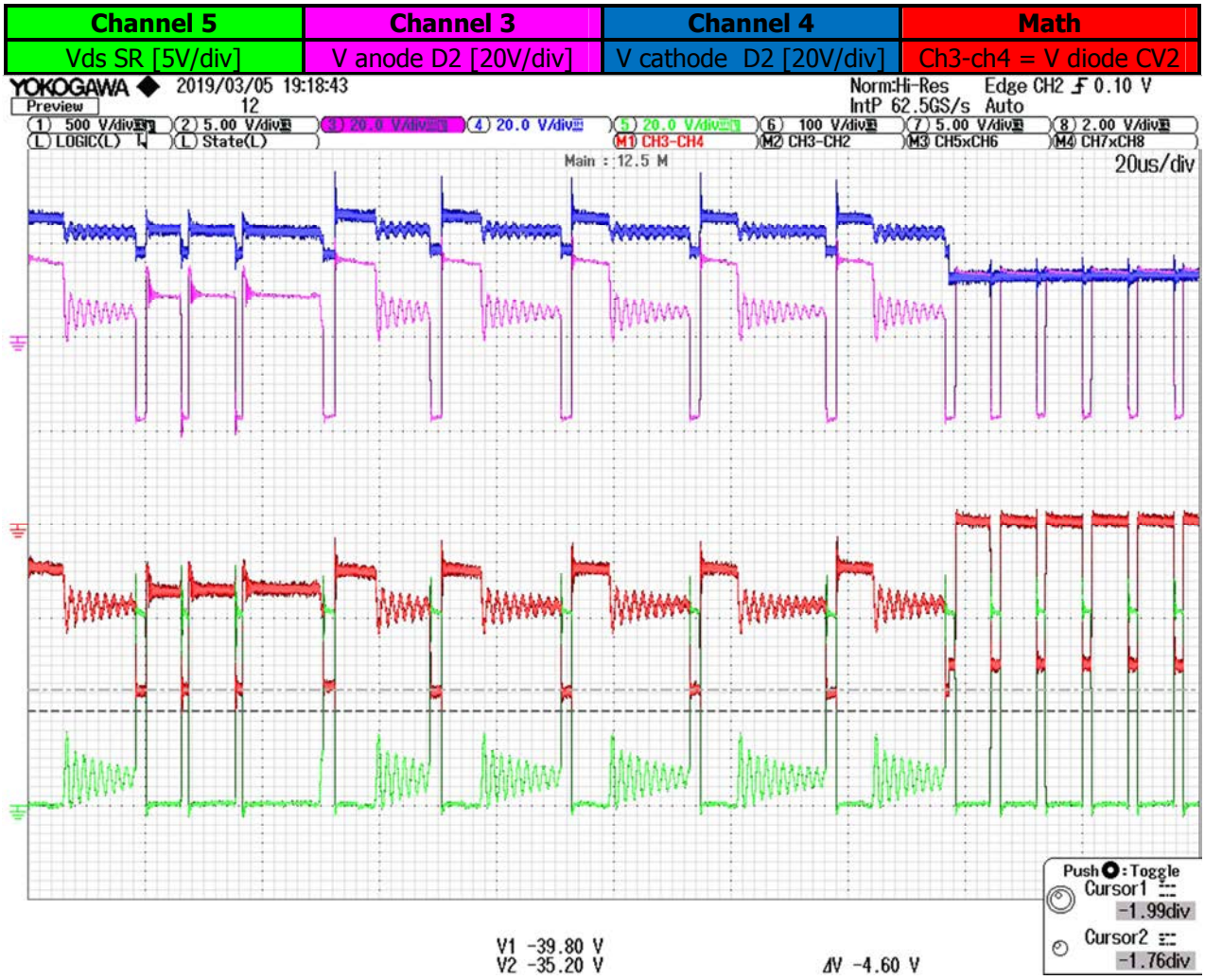


Figure 45 – Voltage on CV2 Diode Under Full Load at 265 VAC.

The maximum reverse voltage across CV2 Diode is <40 V.

12.3.6.5 LED Rectifier Diode Reverse Voltage under Full Load at 265 VAC

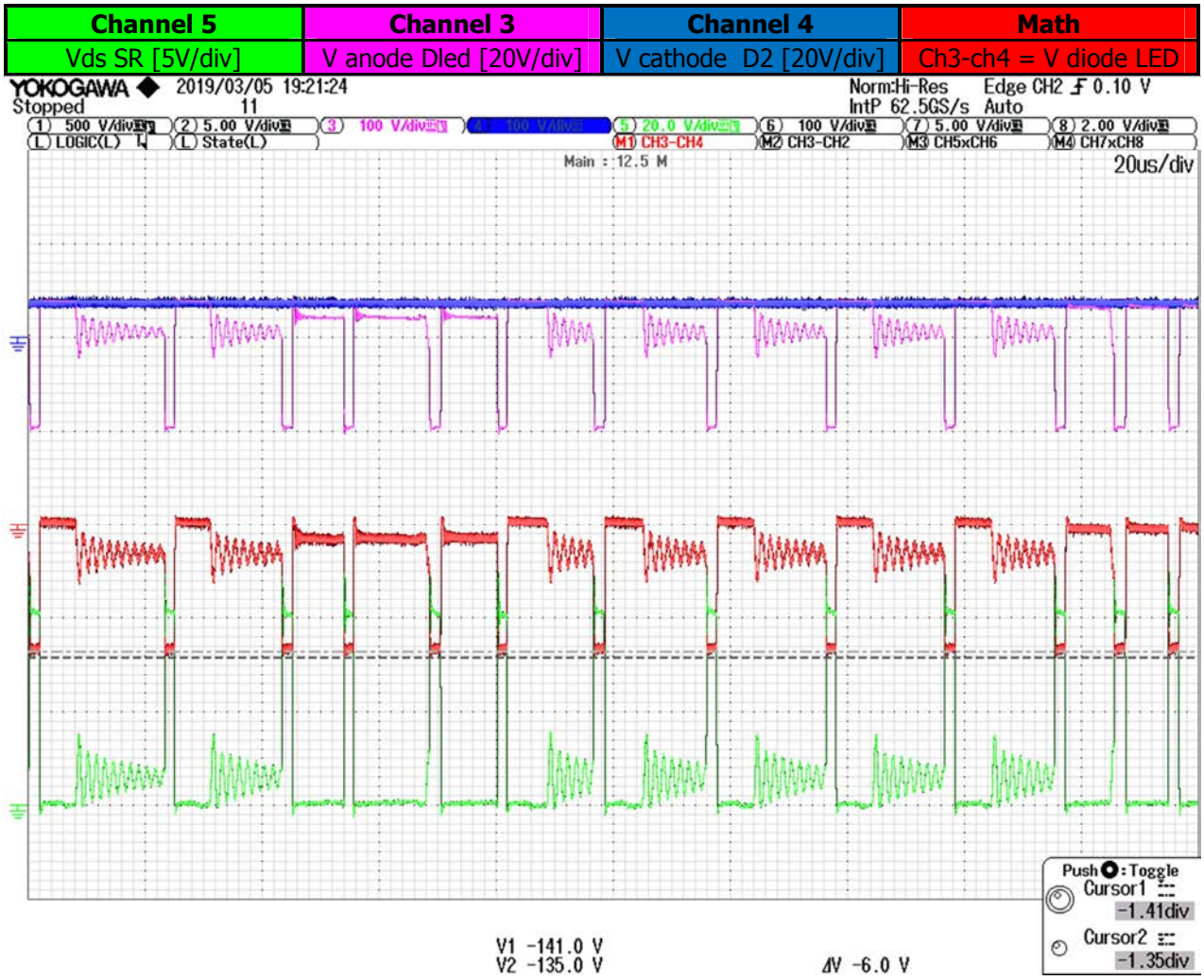


Figure 46 – Voltage on LED Diode Under Full Load at 265 VAC.

The maximum reverse voltage across the LED rectifier diode is <150 V.

12.4 *Brown-In and Brown-Out*

12.4.1 Response at 90 V – 0 V – 90 V

Channel 1	Channel 2	Channel 3	Channel 3
CV1 5 V Output Voltage [V]	AC Input Voltage	LED Output Voltage [V]	CV2 12 V Output Voltage [V]

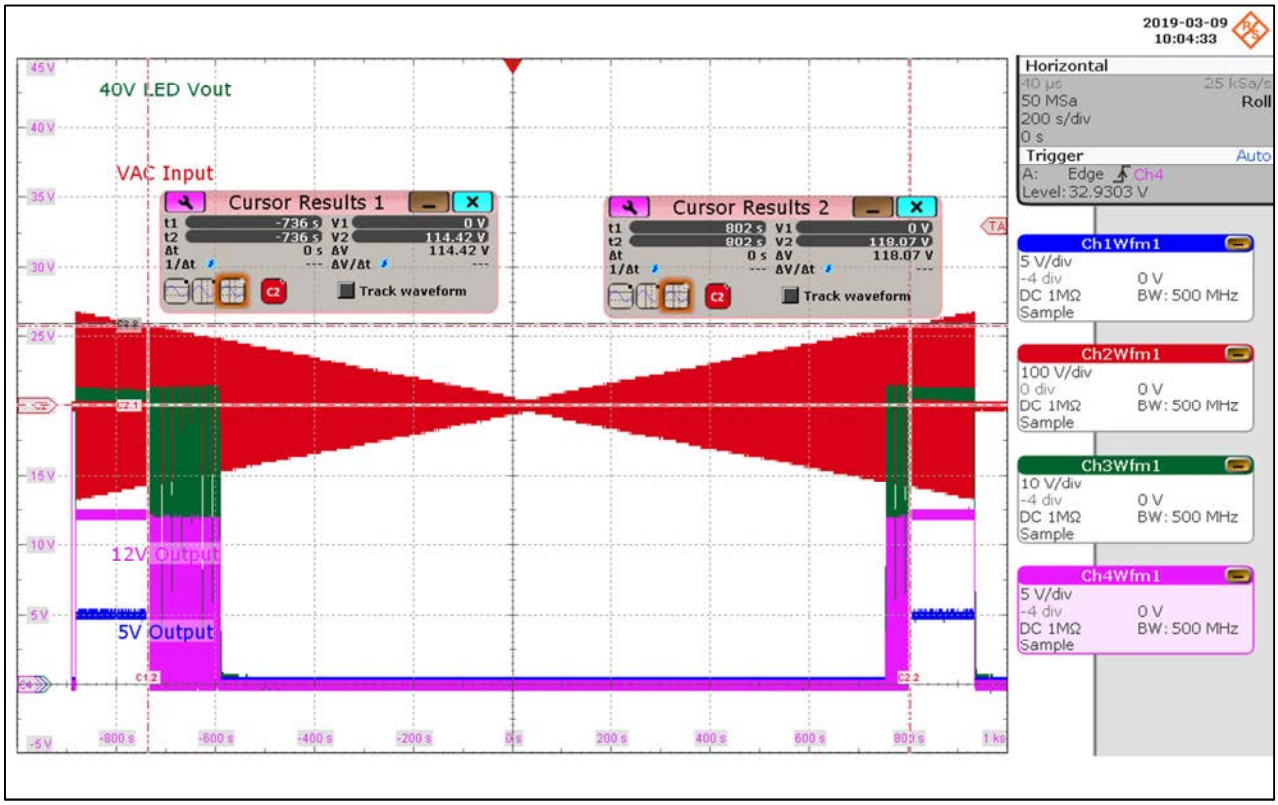


Figure 47 – Brown-In and Brown-Out response, 90 VAC – 0 VAC – 90 VAC.

VAC Input	Brown In Peak Voltage (V_{PK})	Brown In RMS Voltage (V_{RMS})	Brown Out Peak Voltage (V_{PK})	Brown Out RMS Voltage (V_{RMS})
90 VAC	112.33	79.43	113.38	80.17

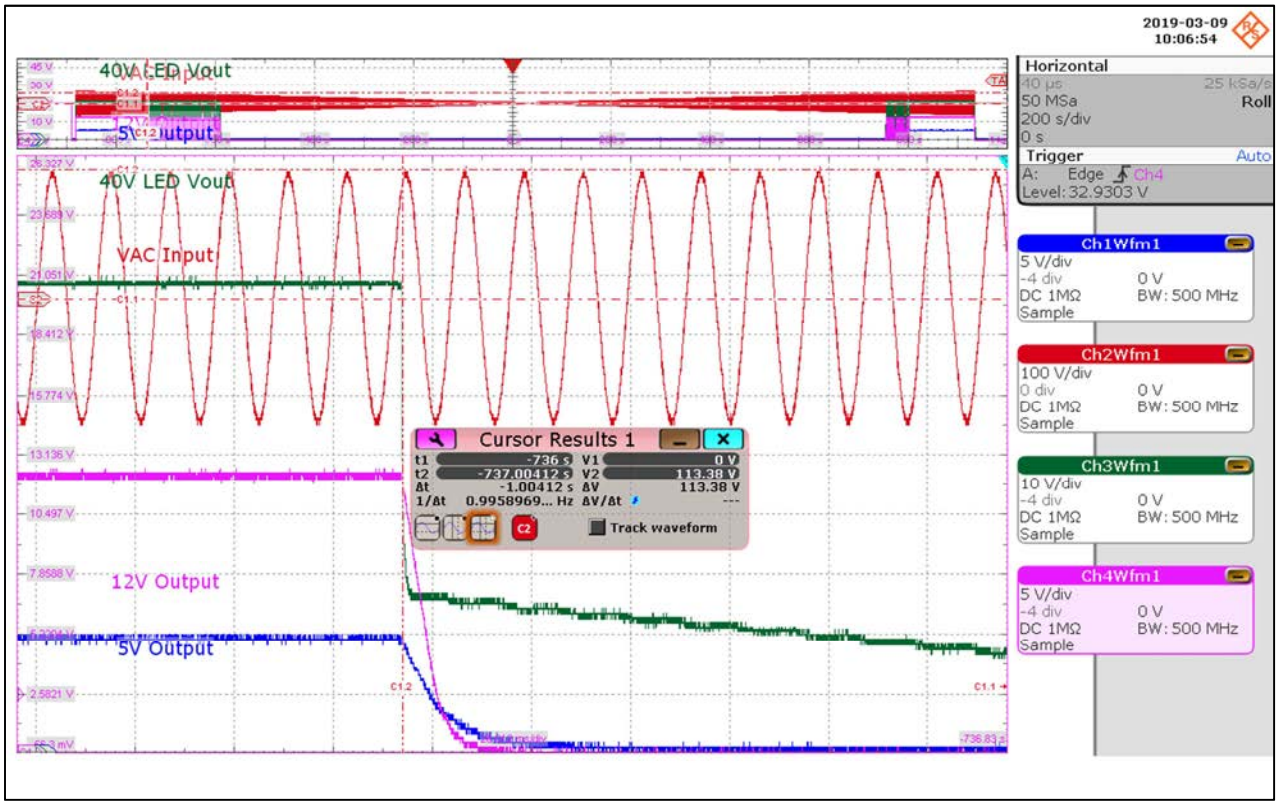


Figure 48 – Brown-Out Response, 90 VAC – 0 VAC – 90 VAC.

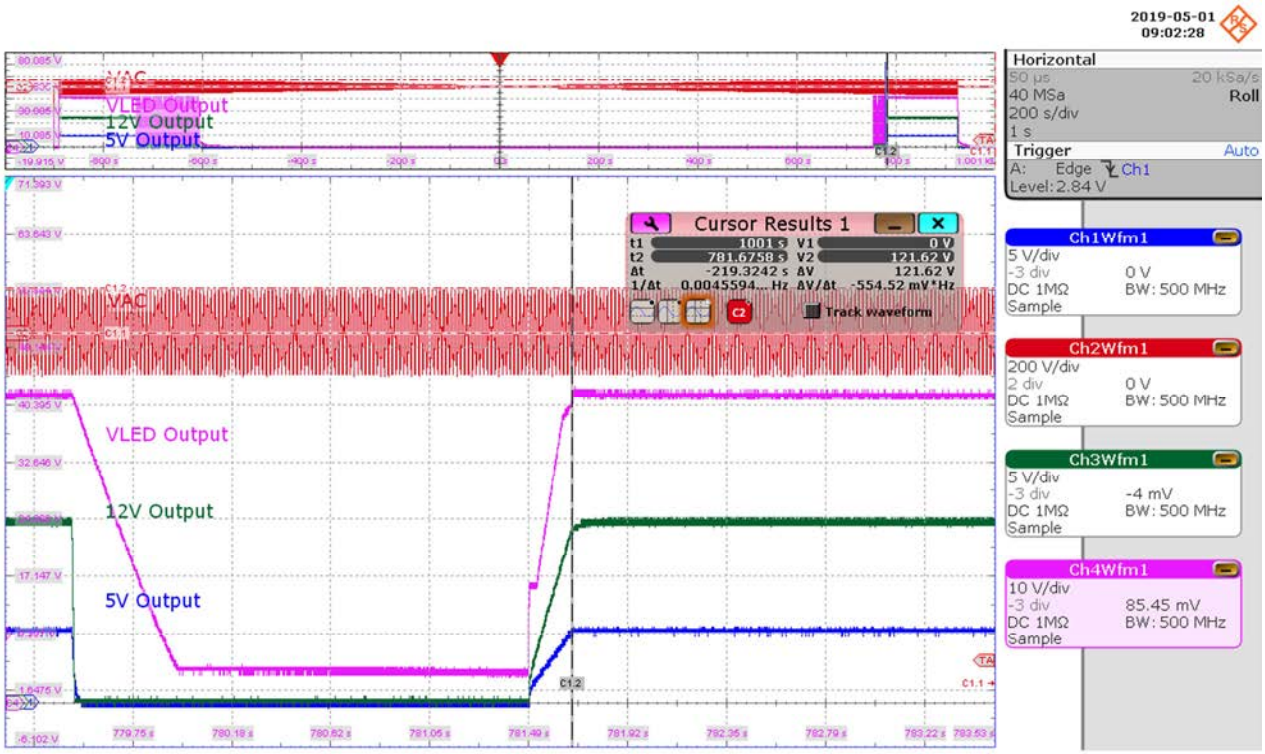


Figure 49 – Brown-In Response, 90 VAC – 0 VAC – 90 VAC.

12.4.2 Response at 265 V – 0 V – 265 V

Channel 1	Channel 2	Channel 3	Channel 3
CV1 5 V Output Voltage [V]	AC Input Voltage	LED Output Voltage [V]	CV2 12 V Output Voltage [V]

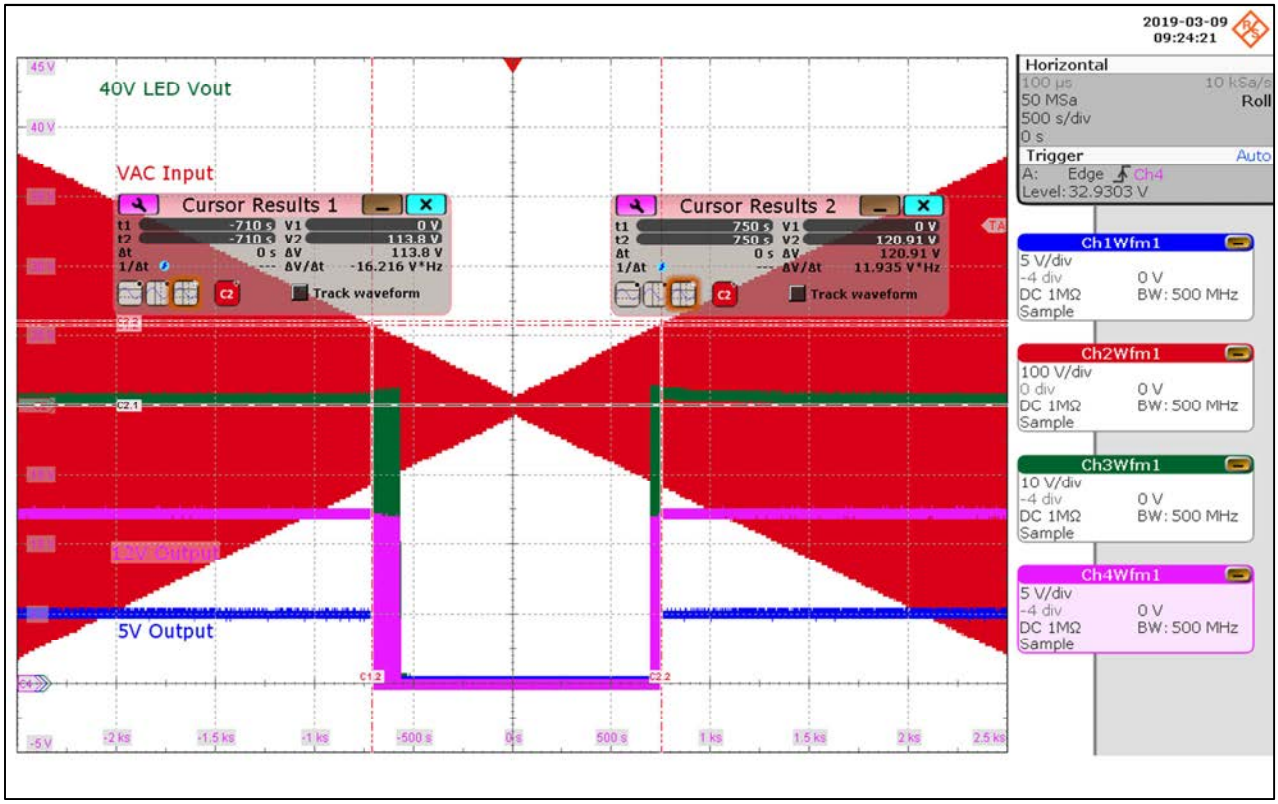


Figure 50 – Brown-In and Brown-Out response, 265 VAC – 0 VAC – 265 VAC.

VAC Input	Brown In Peak Voltage (V_{PK})	Brown In RMS Voltage (V_{RMS})	Brown Out Peak Voltage (V_{PK})	Brown Out RMS Voltage (V_{RMS})
265 VAC	114.42	80.91	113.35	80.15

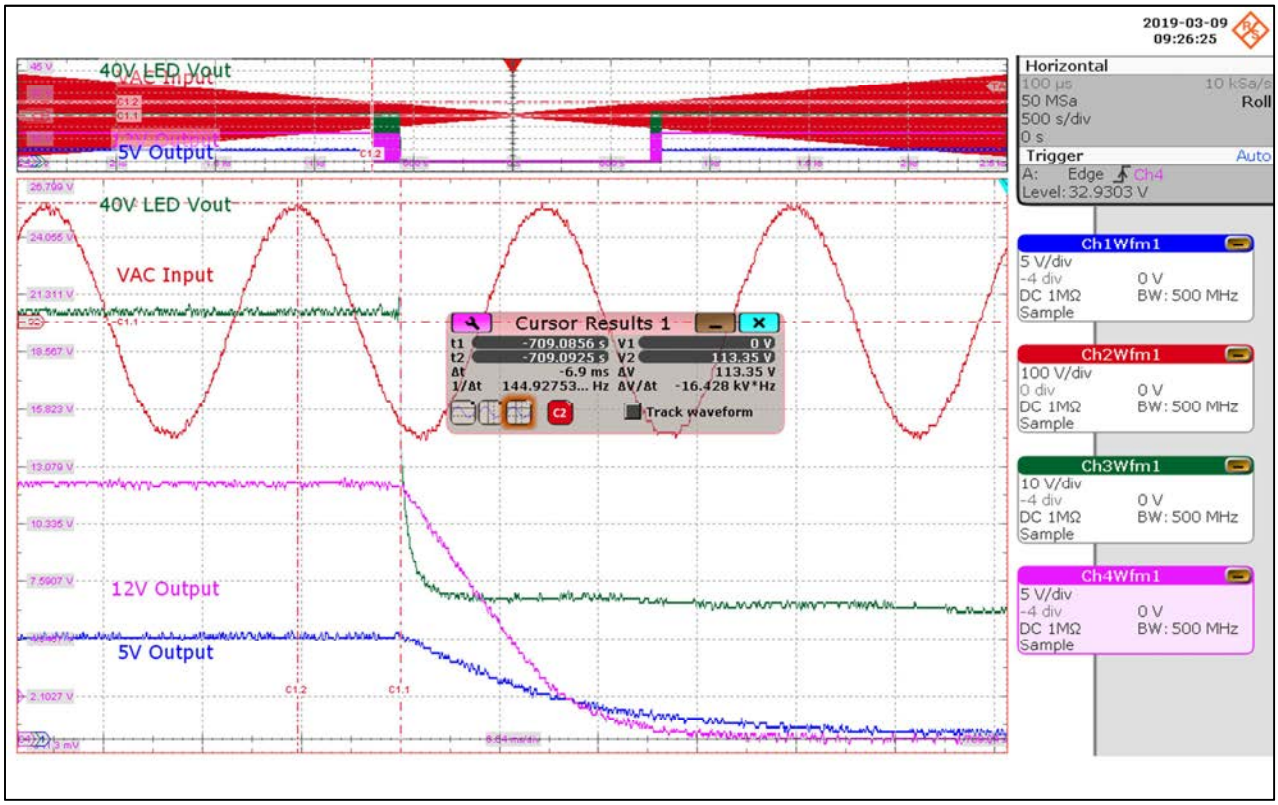


Figure 51 – Brown-Out Response, 265 VAC – 0 VAC – 265 VAC.

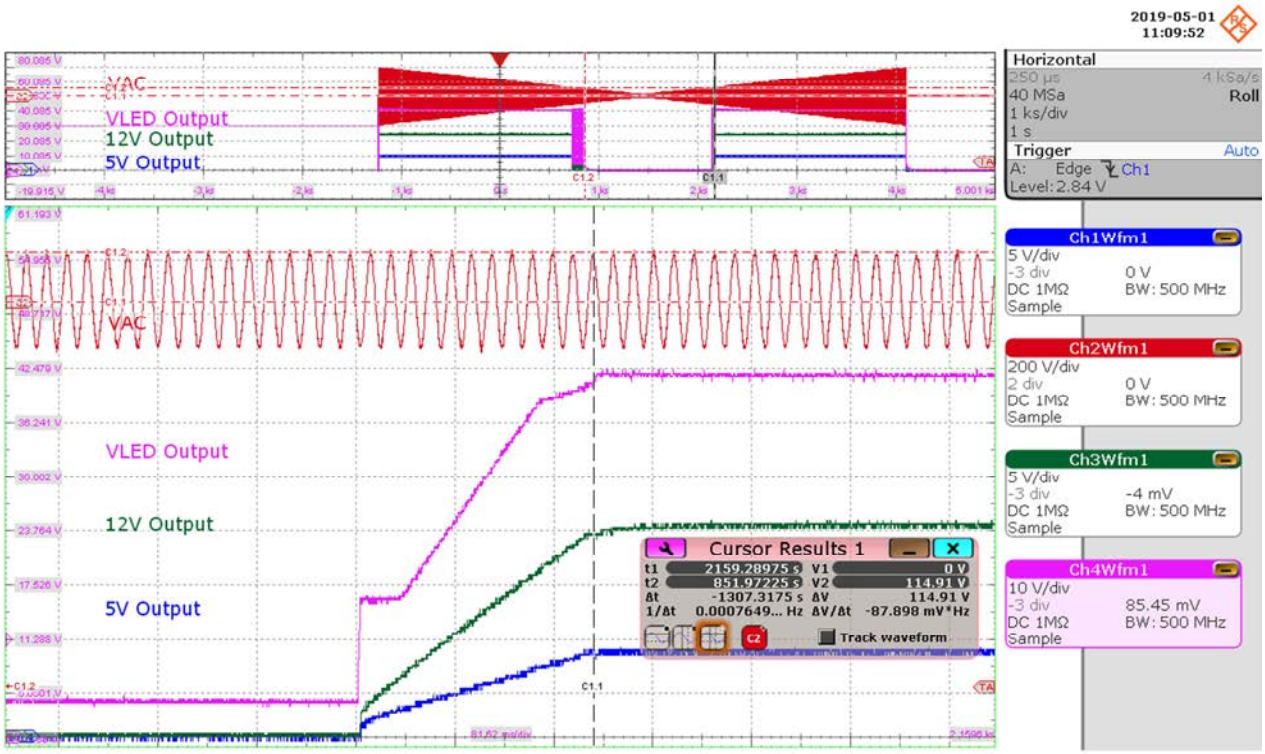


Figure 52 – Brown-In Response, 265 VAC – 0 VAC – 265 VAC.

12.4.3 Response at 0 V – 450 VDC – 0 V

VDC Input	Brown In Peak Voltage (VDC)	Brown In RMS Voltage (V_{RMS})	Brown Out Peak Voltage (VDC)	Brown Out RMS Voltage (V_{RMS})
450 VDC	447.01	316.08 (VAC)	414.02	292.75 (VAC)

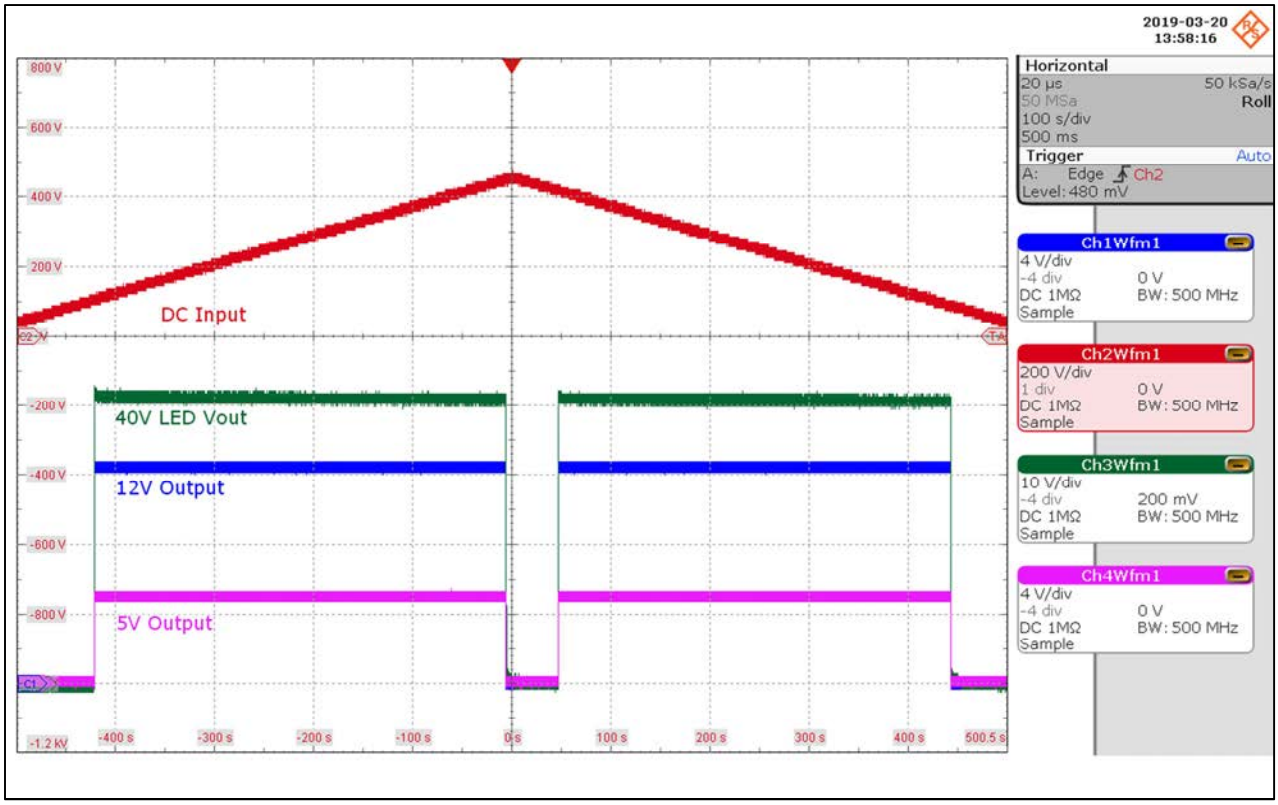


Figure 53 – Brown-In and Brown-Out Response, 0 VDC – 450 VDC – 0 VDC.

12.5 *Overvoltage and Over Current Protections*

12.5.1 CV1 over Voltage and Over Current Protection

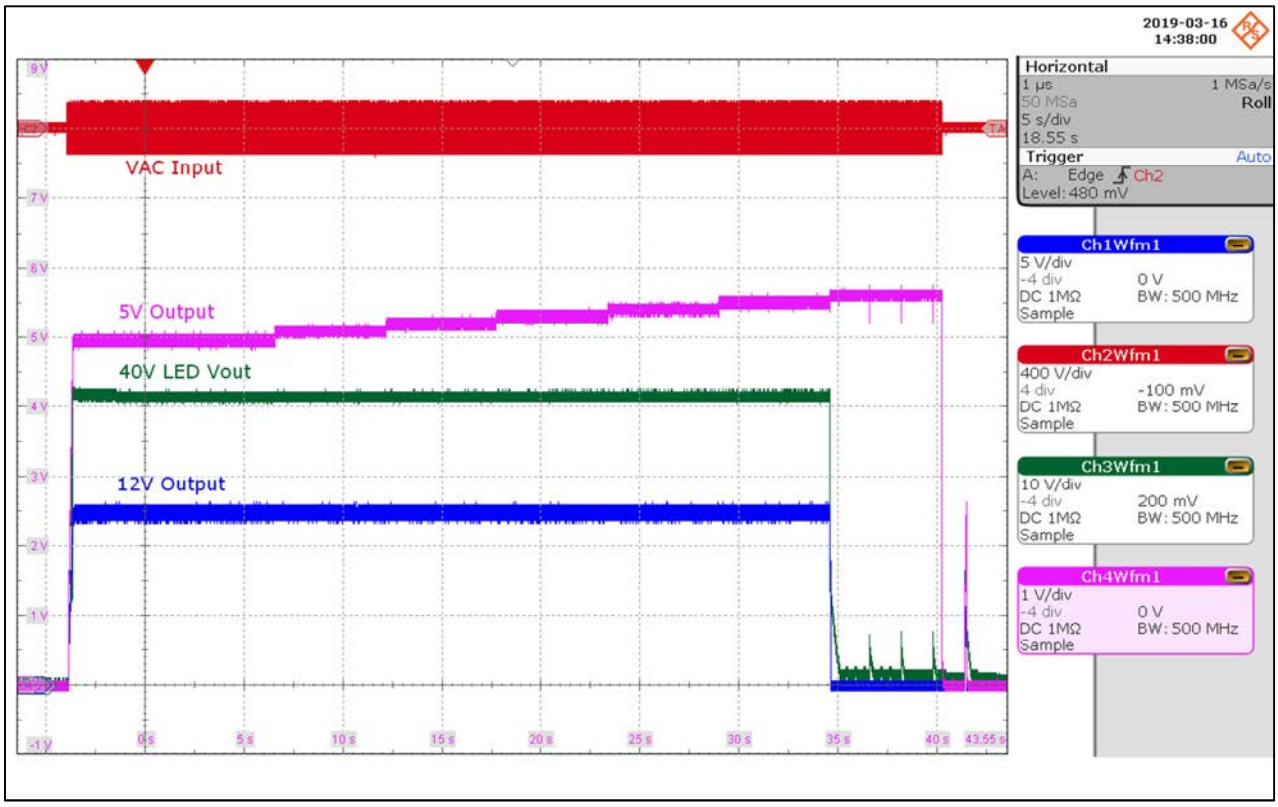


Figure 54 – CV1 Output Overvoltage Protection.

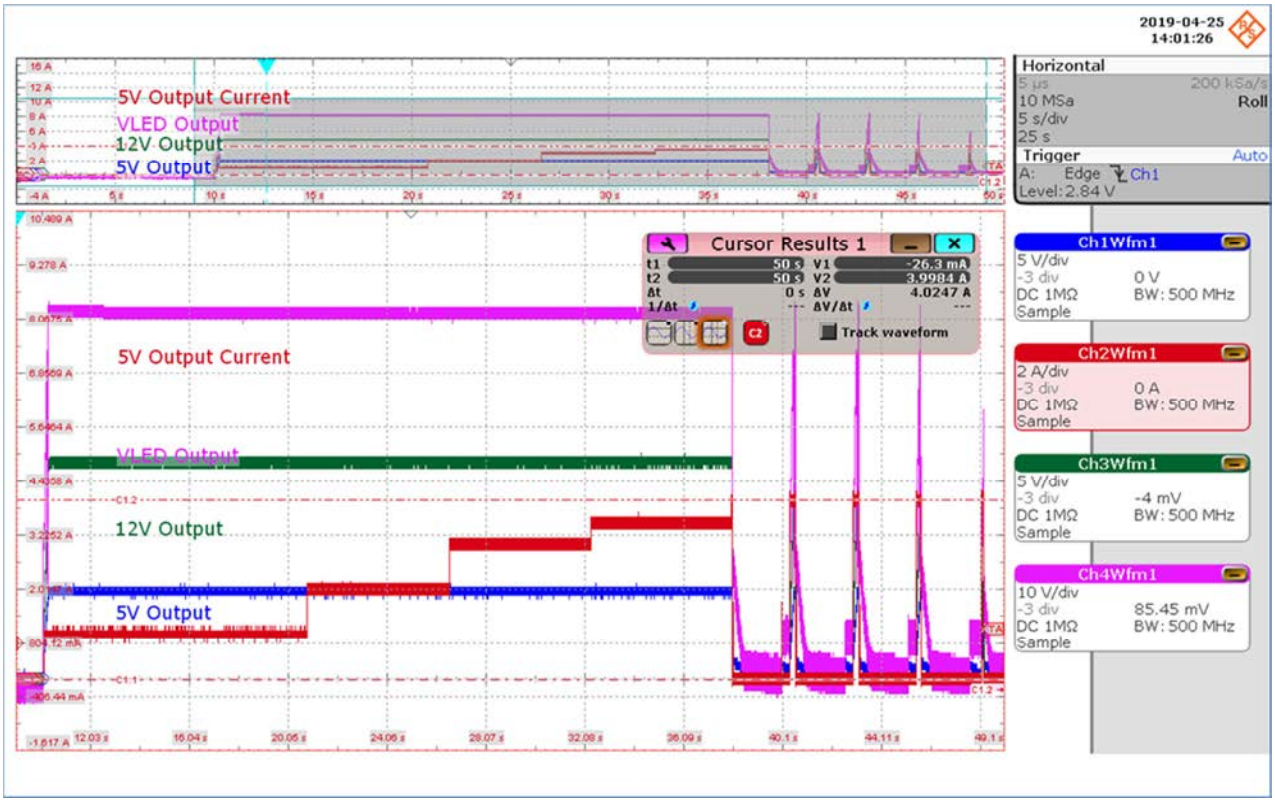


Figure 55 – CV1 Output Over Current Protection.

12.5.2 CV2 OV OC Protections

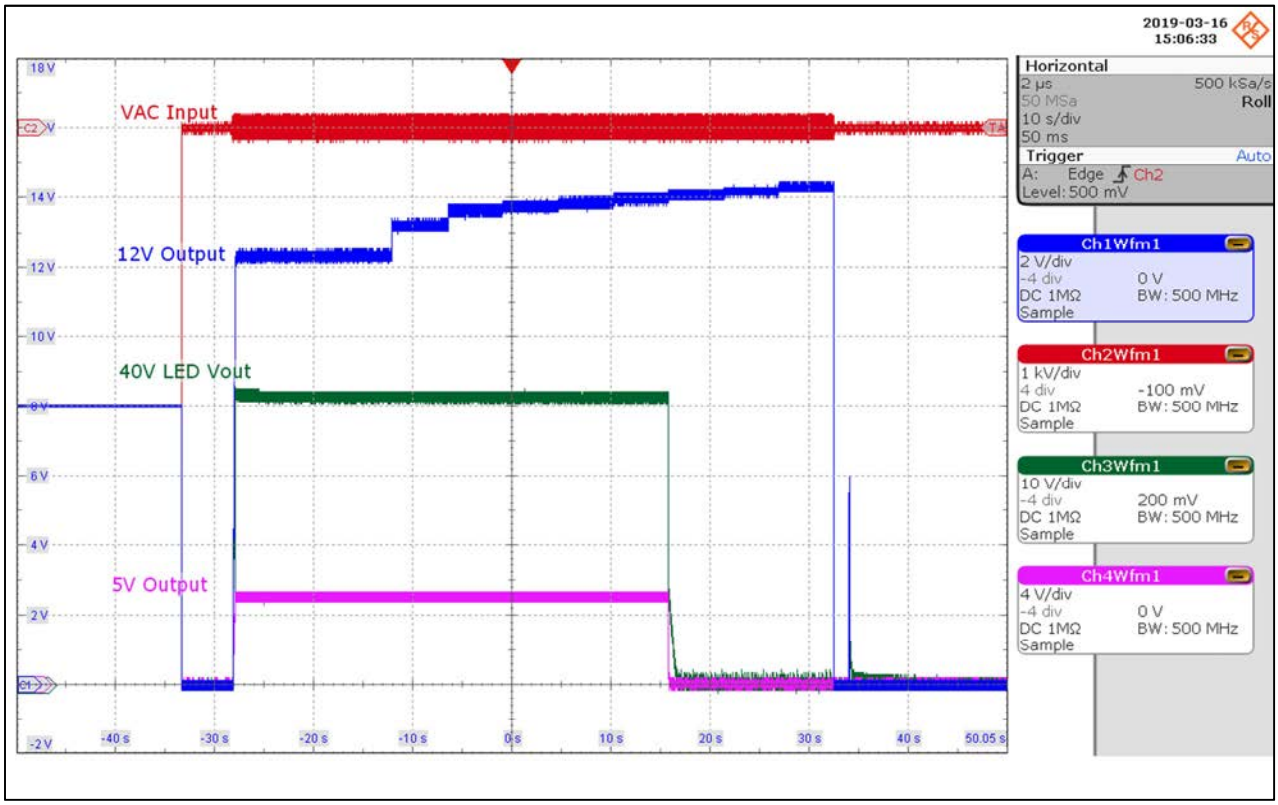


Figure 56 – CV2 Output Overvoltage Protection.

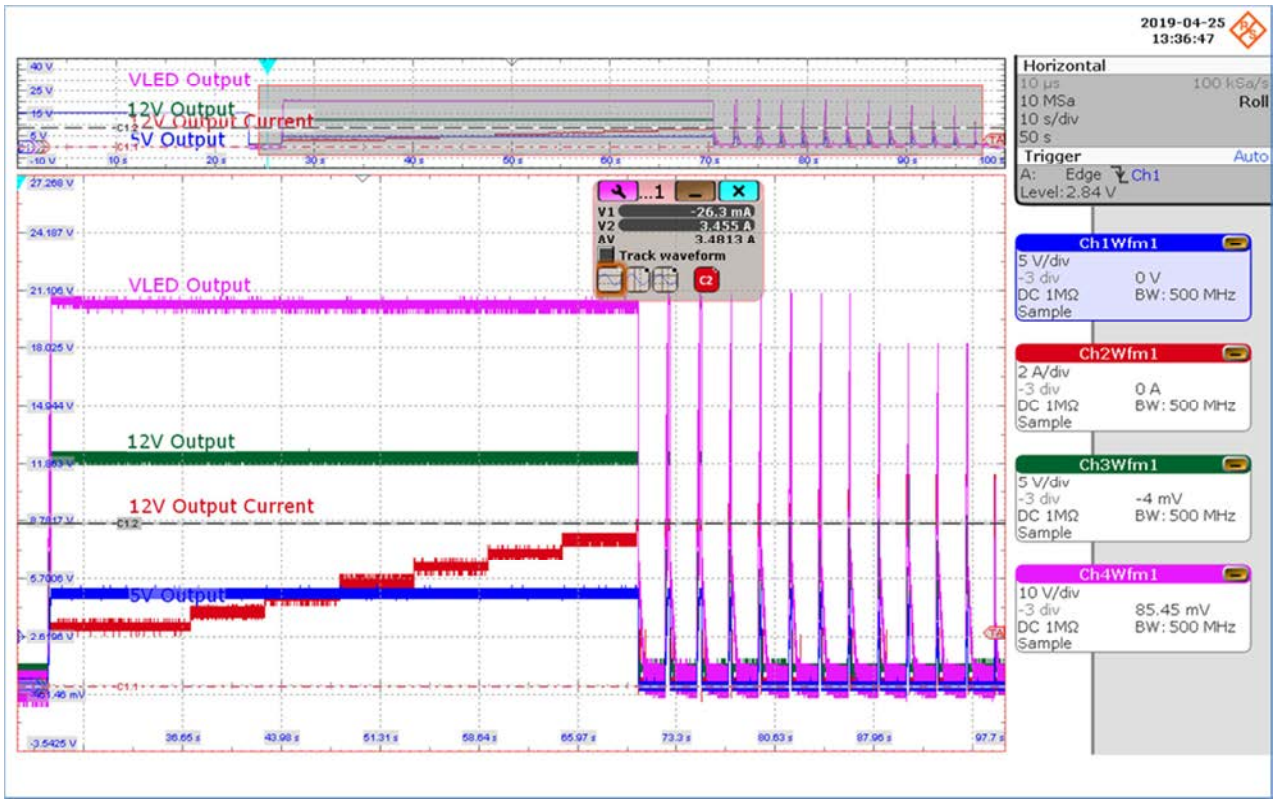


Figure 57 – CV2 Output Over Current Protection.

12.5.3 LED OV OC Protections

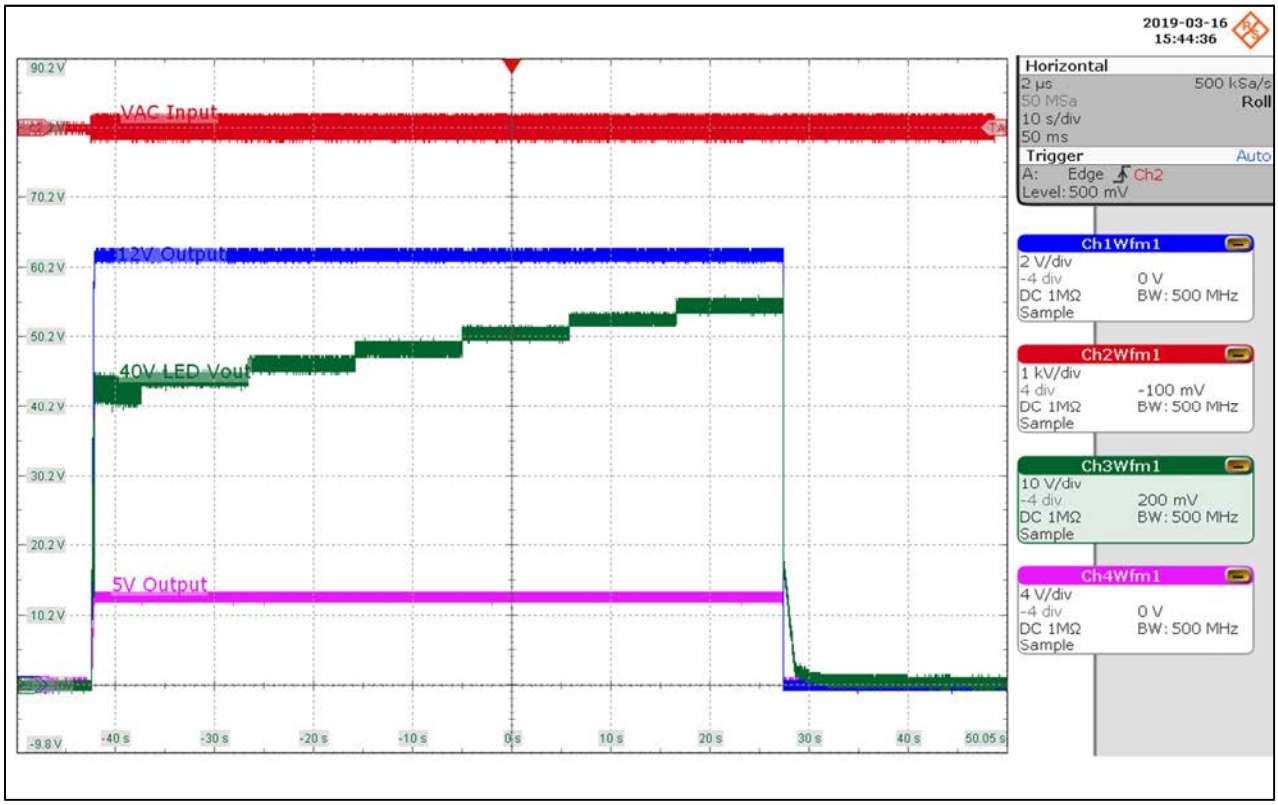


Figure 58 – LED Output Overvoltage Protection.

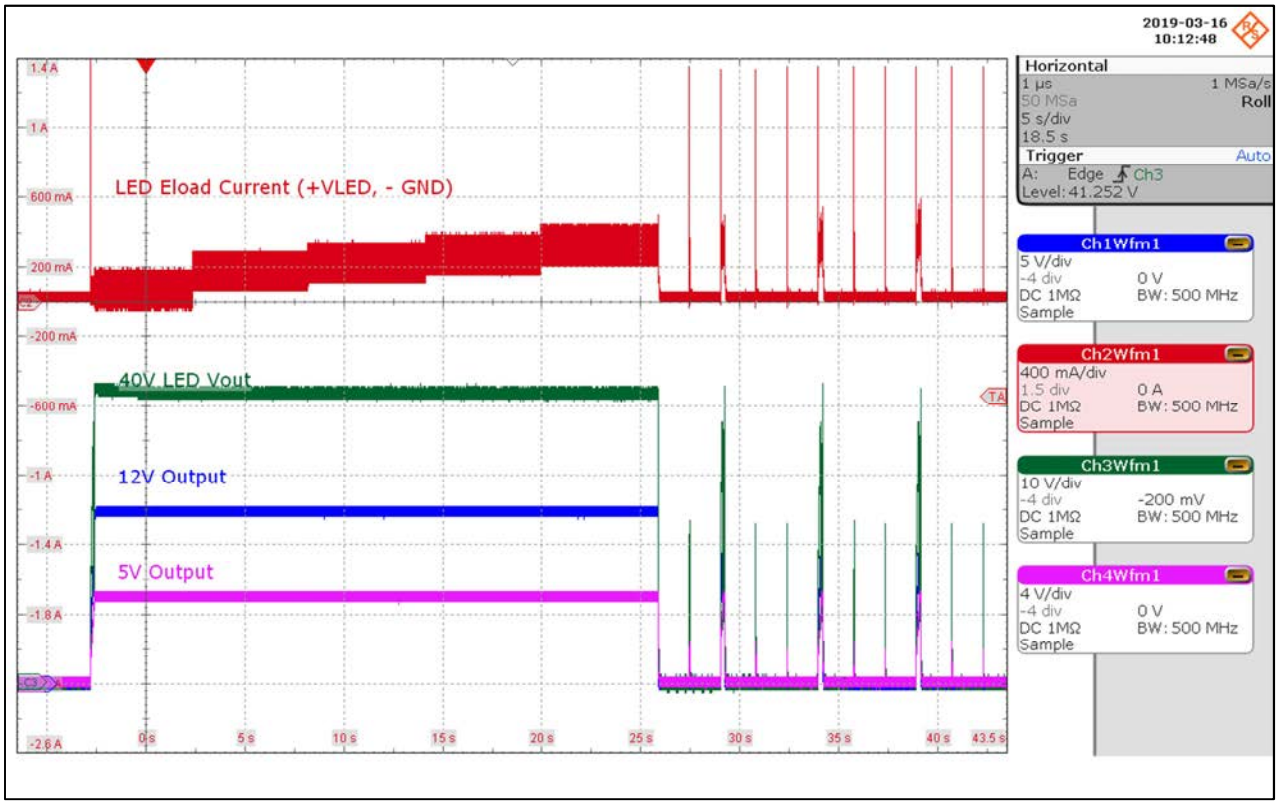


Figure 59 – LED Output over Current Protection.

12.6 *Output Ripple Measurements*

12.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe were utilized in order to reduce noise pick-up. Details of the probe modification are provided in Figure 60.

The probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/100 V ceramic type and one (1) 10 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

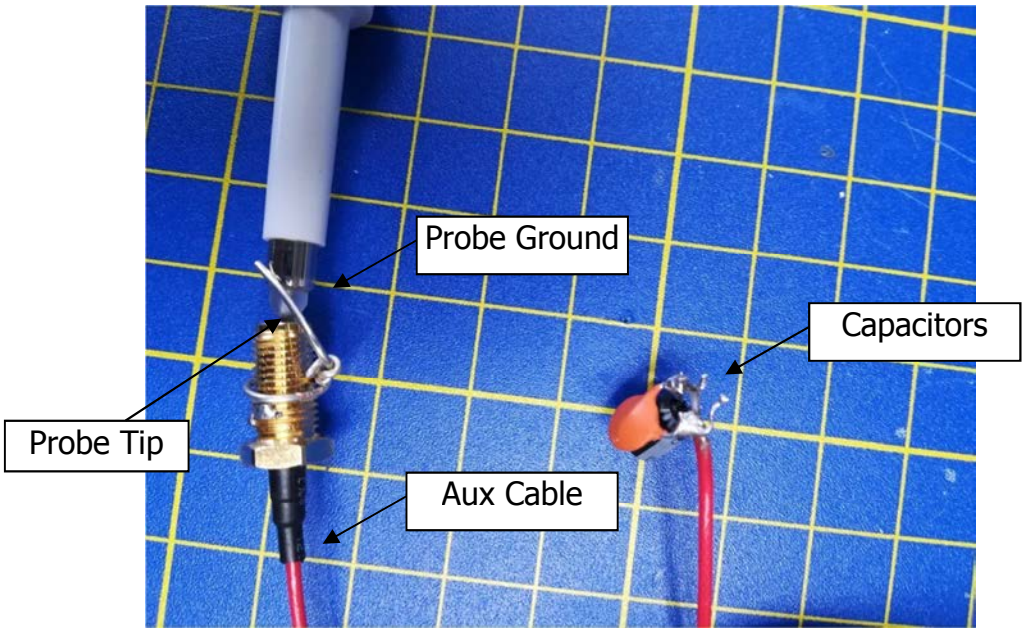


Figure 60 – Oscilloscope Probe Used in Ripple Measurement.

12.6.2 CV1 Output Ripple

Set-up

- 90 VAC – 265 VAC
- Output 5 V @ 5 W, 12 V @ 15 W and LED_40 V @ 25 W
- 20 MHz bandwidth in the scope, 100 nF ceramic capacitor and 10 uF @ 50 V electrolytic capacitor with sniffing connected to output pin

BOM

Level	Value	PN	ESR/Ripple	Size D*L	Quantity
First level	6.3V@1mF polymer	RL80J102MDN1KX	9mOhm/5.7A	8*8	2
Inductance	10uH@3.45A	18R103C	15mOhm	13.7*16	1
Second level	6.3V@1mF	ECA-0JHG102	370mOhm	8*11.5	1
Second level	Ceramic 100nF	VJ1206Y104KXCAT		1206	

Table 9 – 5 V Filter BOM.

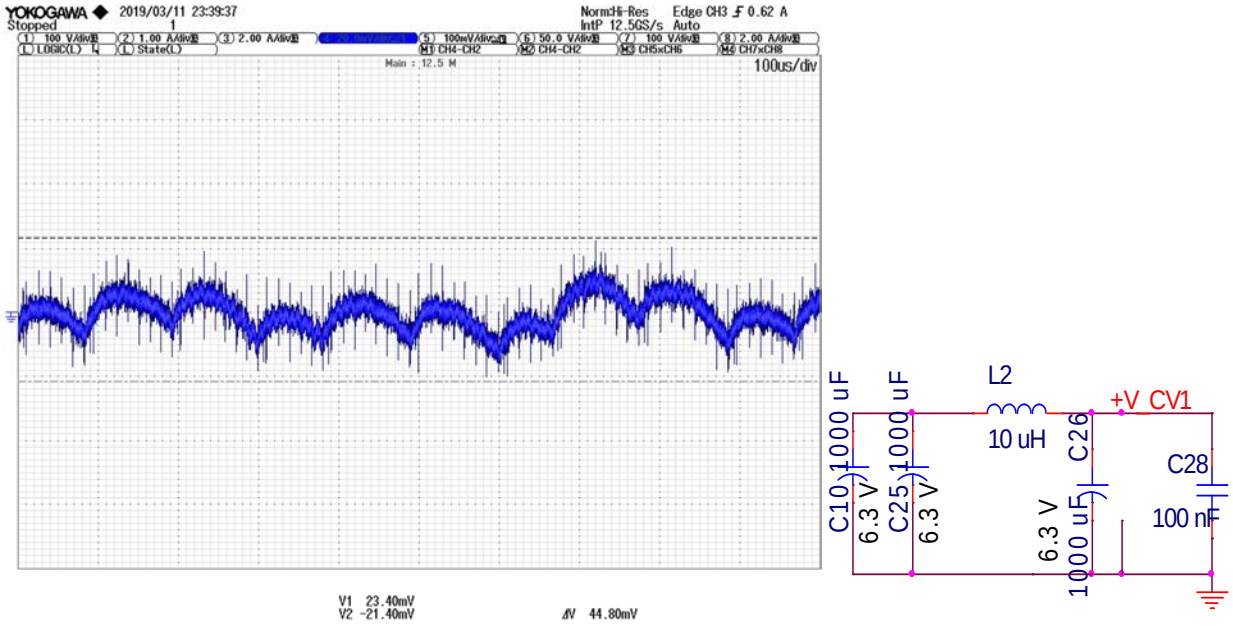


Figure 61 – Vo1 Ripple Waveform.

Result – 44.8 mV ripple

12.6.3 CV2 Output Ripple

Set-up

- 90 VAC – 265 VAC
- Output 5 V @ 5 W, 12 V @ 15 W and LED_40 V @ 25 W
- 20 MHz bandwidth in the scope, 100 nF ceramic capacitor and 10 uF @ 50 V electrolytic capacitor with sniffing connected to output pin

BOM

Level	Value	PN	ESR/Ripple	Size D*L	Quantity
First level	16V@470uF polymer	RNE1C471MDN1	10mOhm/5.4A	8*11.5	1
Inductance	10uH@3.45A	18R103C	15mOhm	13.7*16	1
Second level	16V@680uF	EZKE160ELL681MH20D	69mOhm/1.25A	8*20	2
Second level	Ceramic 100nF	VJ1206Y104KXCAT		1206	1

Table 10 – 12 V Filter BOM.

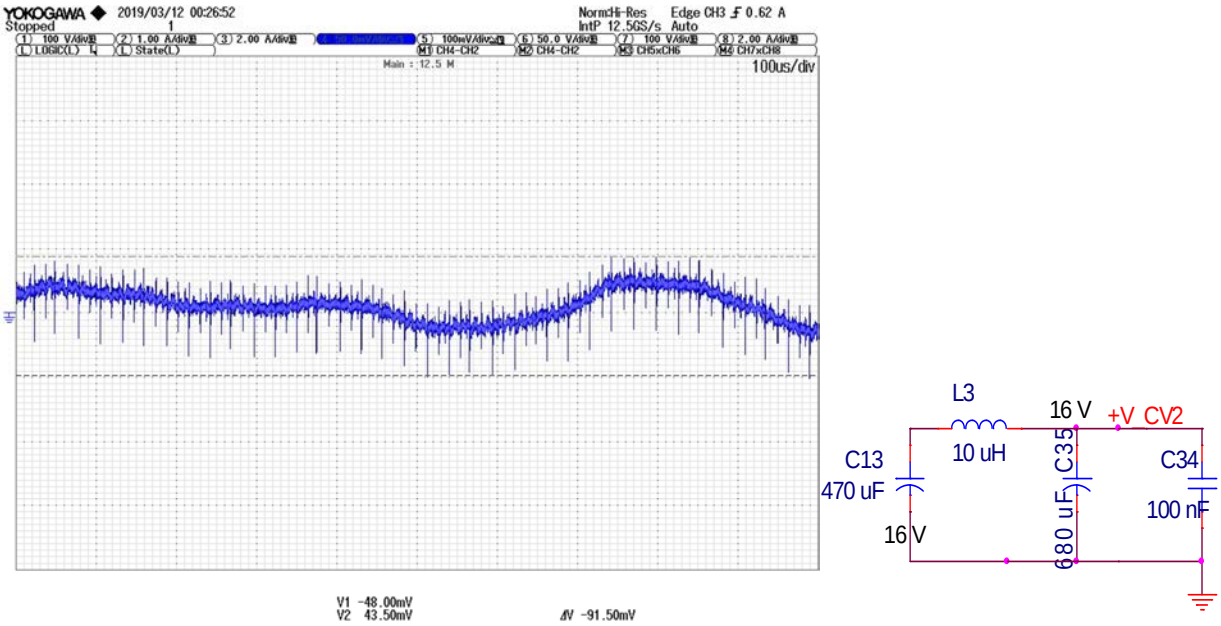


Figure 62 – Vo2 Ripple Waveform.

Result – 91.5 mV ripple

12.7 *LED output*

Setup

- 90 VAC – 265 VAC
- Output 5 V @ 5 W, 12 V @ 15 W and LED_40 V @ 25 W
- 20 MHz bandwidth in the scope, measured current

BOM

Level	Value	PN	ESR/Ripple	Size D*L	Quantity
First level	63V@56uF polymer	KMG10WV1000UF10X12.5	25mOhm/2.6A	10*12.5	1
Inductance	Non				
Second level	63V@120uF polymer	EKZE06303121MH20D	120mOhm/0.82	8*20	1
Second level	Ceramic 100nF	VJ1206Y104KXCAT		1206	1

Table 11 – LED filter BOM

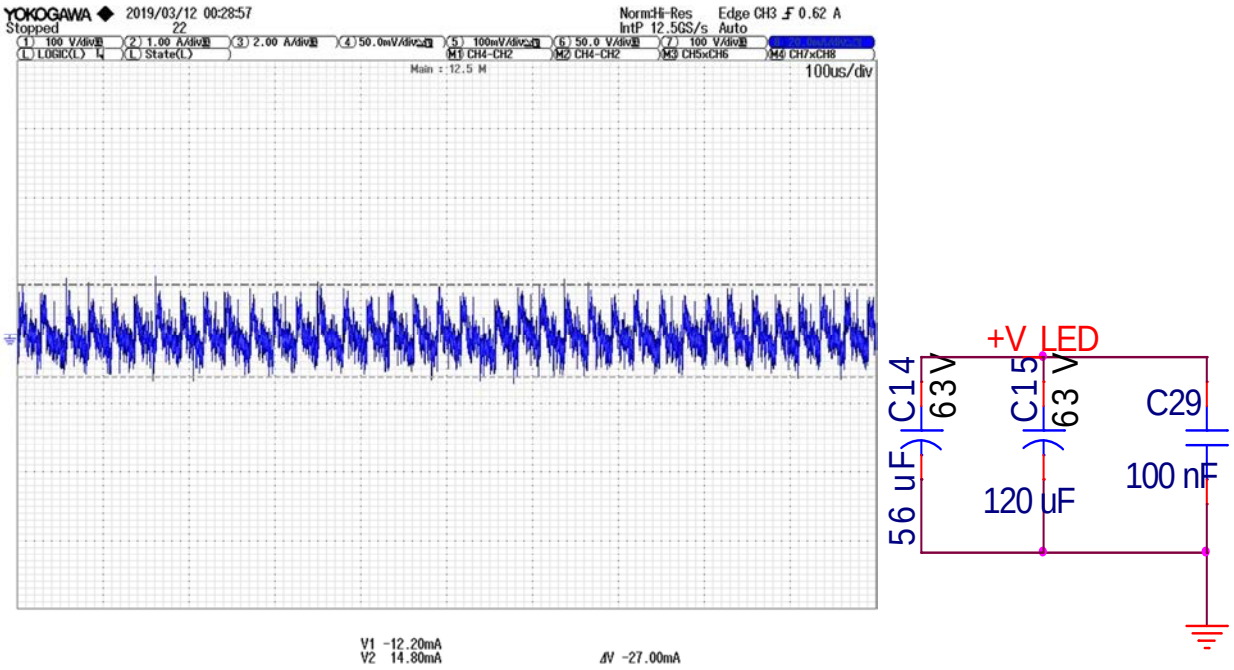


Figure 63 – LED Ripple Waveform.

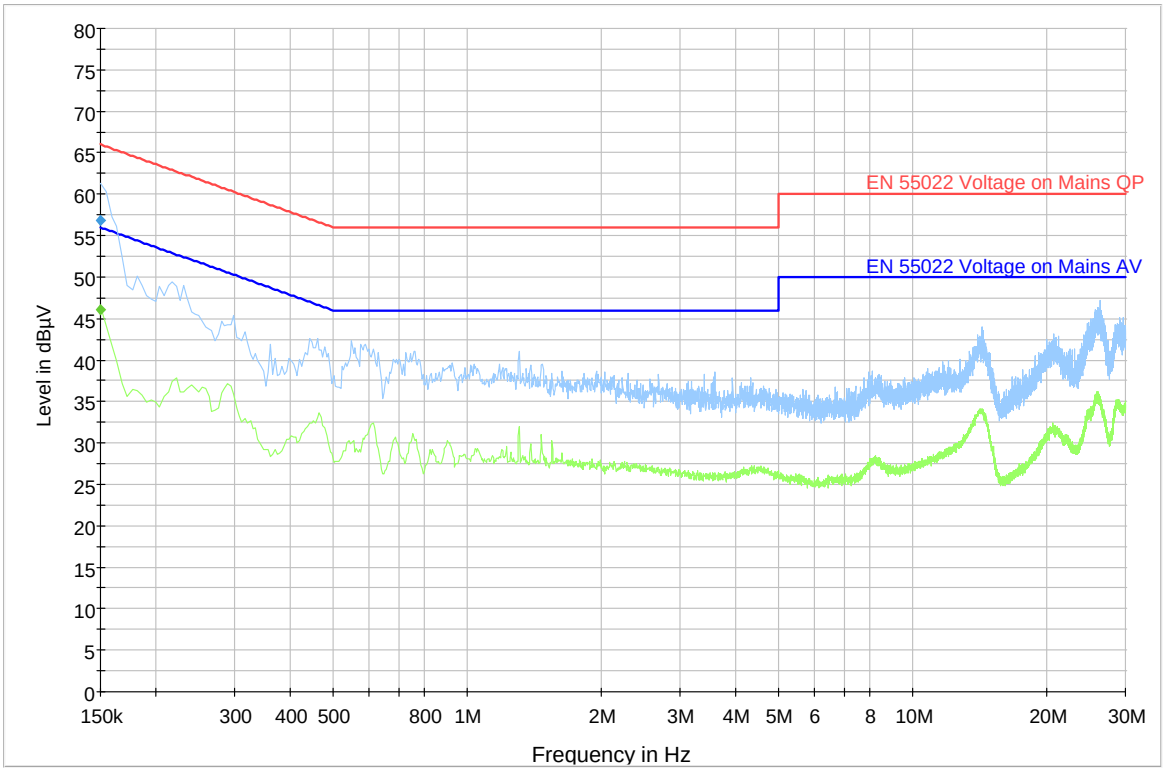
Result – 27 mA ripple

13 Conducted EMI

With worst case test results, there is still 9.2dB minimum margin.

- PSU GND is connected to earth (PE)
- Full load

13.1 *115 VAC*



Final Measurement Detector 1

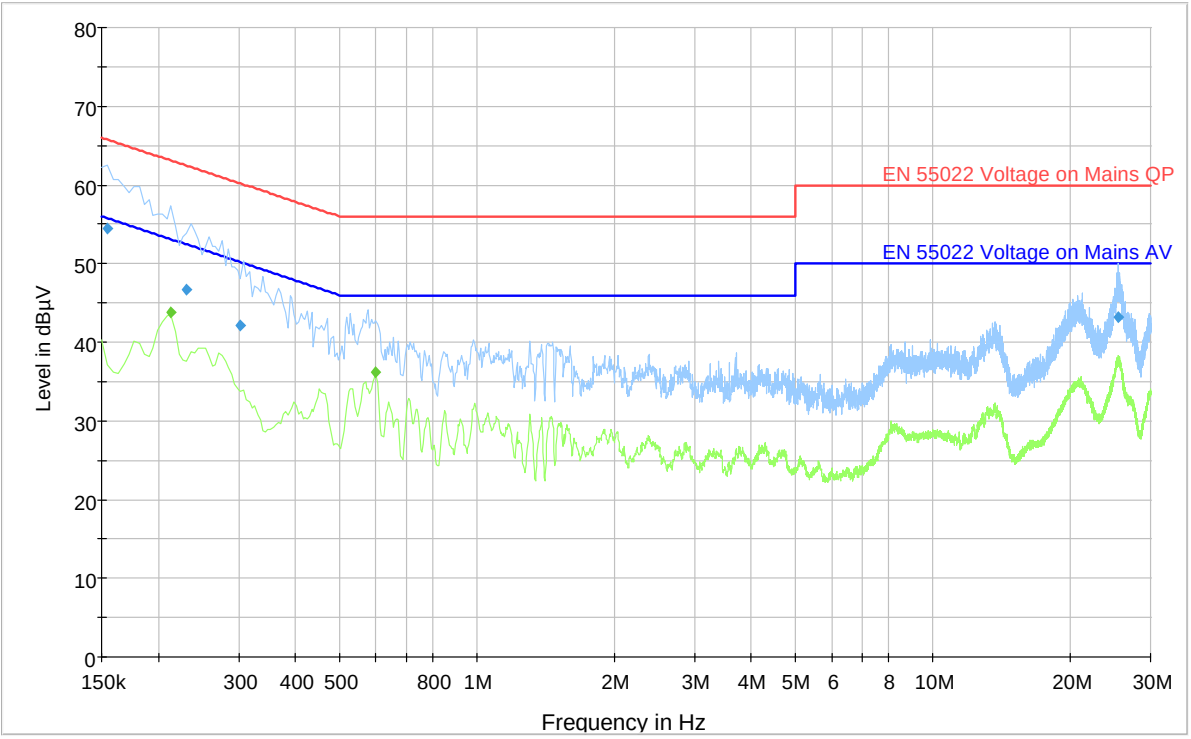
Frequency (MHz)	QuasiPeak (dBµV)	Meas. Time (ms)	Bandwidth (kHz)	Filter	Line	Corr. (dB)	Margin (dB)	Limit (dBµV)	Comment
0.150000	56.8	1000.000	10.000	On	N	20.0	9.2	66.0	

Final Measurement Detector 2

Frequency (MHz)	Average (dBµV)	Meas. Time (ms)	Bandwidth (kHz)	Filter	Line	Corr. (dB)	Margin (dB)	Limit (dBµV)	Comment
0.150000	46.1	1000.000	10.000	On	L1	20.0	9.9	56.0	

Figure 64 – EMI Test Results at 115 V.

13.2 *230 VAC*



Final Measurement Detector 1

Frequency (MHz)	QuasiPeak (dBµV)	Meas. Time (ms)	Bandwidth (kHz)	Filter	Line	Corr. (dB)	Margin (dB)	Limit (dBµV)	Comment
0.154500	54.5	1000.000	10.000	On	L1	20.0	11.3	65.8	
0.230500	46.6	1000.000	10.000	On	L1	20.0	15.8	62.4	
0.302500	42.2	1000.000	10.000	On	N	20.0	18.0	60.2	
25.503500	43.2	1000.000	10.000	On	L1	20.0	16.8	60.0	

Final Measurement Detector 2

Frequency (MHz)	Average (dBµV)	Meas. Time (ms)	Bandwidth (kHz)	Filter	Line	Corr. (dB)	Margin (dB)	Limit (dBµV)	Comment
0.212500	43.8	1000.000	10.000	On	N	20.0	9.3	53.1	
0.599500	36.2	1000.000	10.000	On	N	20.0	9.8	46.0	

Figure 65 – EMI Test Results at 230 V.

14 ESD Test

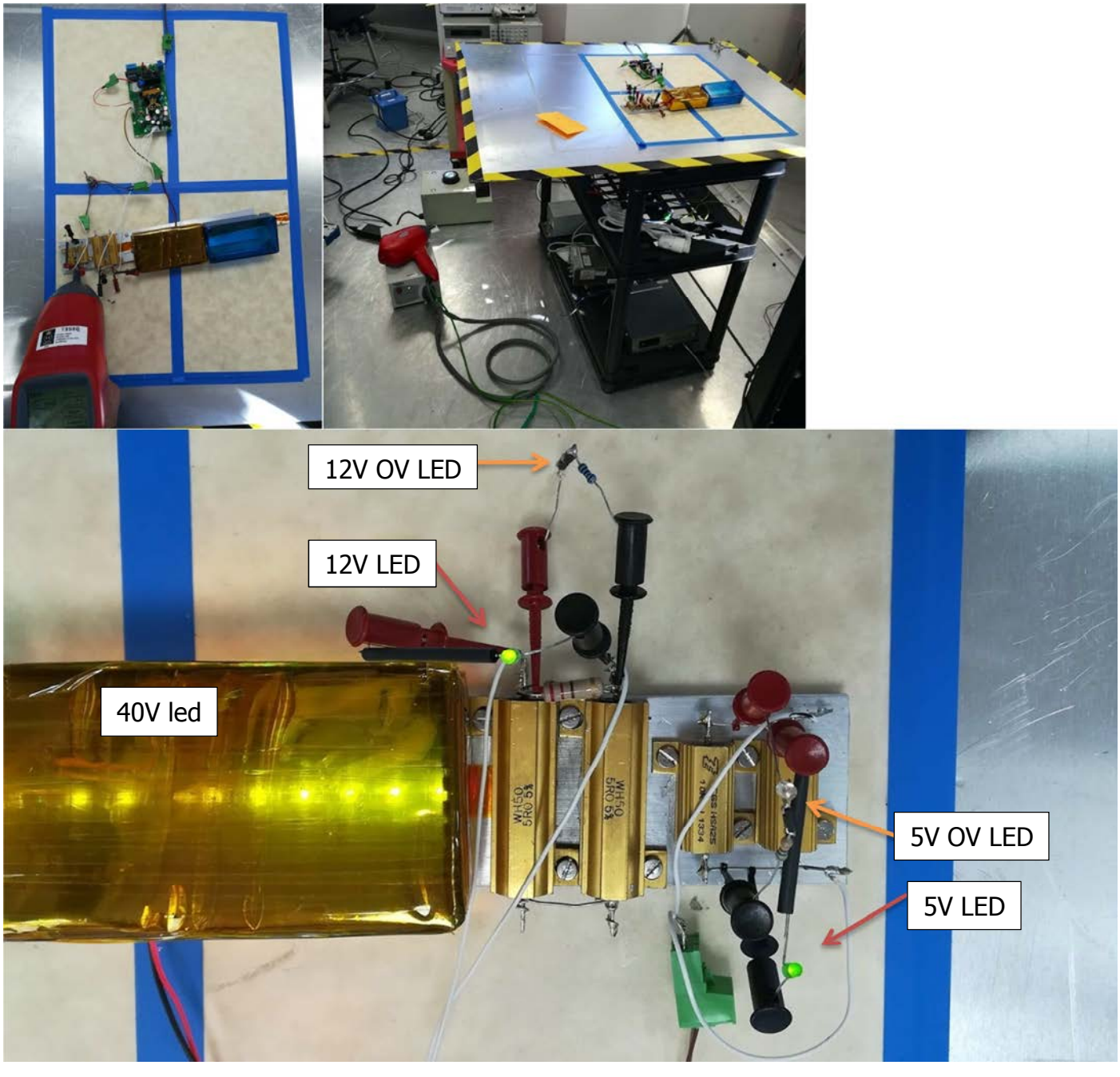


Figure 66 – ESD Set-Up.

14.1 *ESD contact pulse on the PSU GND.*

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result (Pass/Fail)
2000	230	Contact	10	Pass
-2000	230	Contact	10	Pass
4000	230	Contact	10	Pass
-4000	230	Contact	10	Pass
6000	230	Contact	10	Pass
-6000	230	Contact	10	Pass
8000	230	Contact	10	Pass
-8000	230	Contact	10	Pass
8800	230	Contact	10	Pass
-8800	230	Contact	10	Pass

Table 12 – ESD Contact Discharge Test.

14.2 *ESD Air discharge pulse on the PSU GND.*

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result (Pass/Fail)
2000	230	Air	10	Pass
-2000	230	Air	10	Pass
4000	230	Air	10	Pass
-4000	230	Air	10	Pass
8000	230	Air	10	Pass
-8000	230	Air	10	Pass
15000	230	Air	10	Pass
-15000	230	Air	10	Pass
16500	230	Air	10	Pass
-16500	230	Air	10	Pass

Table 13 – ESD Air Discharge Test.

15 Surge Test

Surge pulse between L-N with 2 Ω resistance.

Ring Wave Voltage (kV)	Phase Angle (°)	V measured (V)	I measured (A)	Number of Strikes	Test Result
1	0	769	127	10	PASS
-1	0	-789	-145	10	PASS
1	90	916	249	10	PASS
-1	90	-642	-120	10	PASS
1	180	795	147	10	PASS
-1	180	-796	-123	10	PASS
1	270	650	123	10	PASS
-1	270	-908	-237	10	PASS

Table 14 – Surge L-N Test.

Surge pulse between L-PE with 12 Ω resistance.

Ring Wave Voltage (kV)	Phase Angle (°)	V measured (V)	I measured (A)	Number of Strikes	Test Result
2	0	1927	54	10	PASS
-2	0	-1912	-29	10	PASS
2	90	2246	63	10	PASS
-2	90	-1568	-25A	10	PASS
2	180	1900	54	10	PASS
-2	180	-1895	-26	10	PASS
2	270	1601	47	10	PASS
-2	270	-2223	-31	10	PASS

Table 15 – Surge L-PE Test.

Surge pulse between N-PE with 12 Ω resistance.

Ring Wave Voltage (kV)	Phase Angle (°)	V measured (V)	I measured (A)	Number of Strikes	Test Result
2	0	1918	59	10	PASS
-2	0	-1901	-29	10	PASS
2	90	1914	54	10	PASS
-2	90	-1917	-29	10	PASS
2	180	1924	59	10	PASS
-2	180	-1888	-26	10	PASS
2	270	1910	65	10	PASS
-2	270	-1901	-25	10	PASS

Table 16 – Surge N-PE Test.

16 Thermal Performance

16.1 *Cooling Assembly*

Aluminum plate 64.7 mm x 70 mm x 1.2 mm with holes and thermal pad of 17.5 mm x 16 mm, second layer is 70.7 mm x 76 mm Nomex Isolation with plastic screws and 2.4 mm washers. The hole is exactly the chip size 10.3 mm x 9.4 mm.

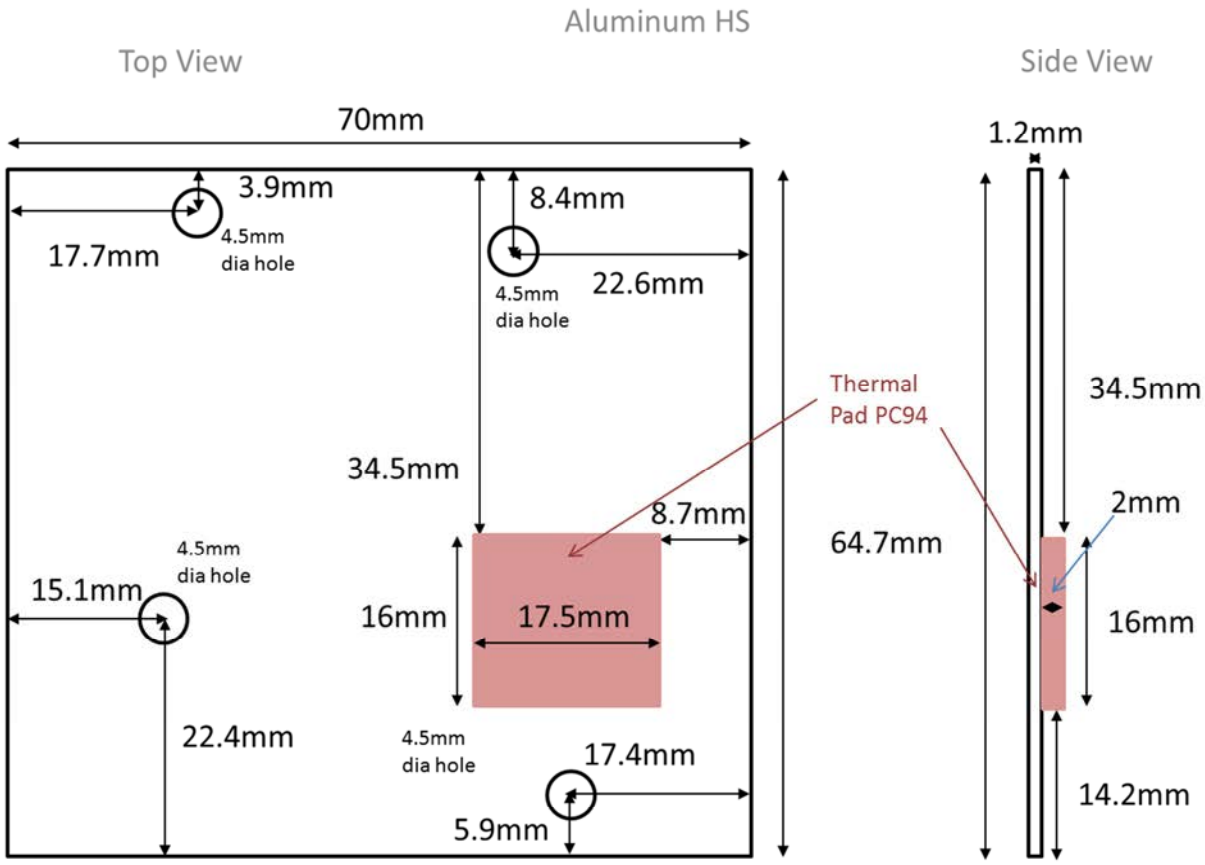


Figure 67 – Heat Sink Dimensions.

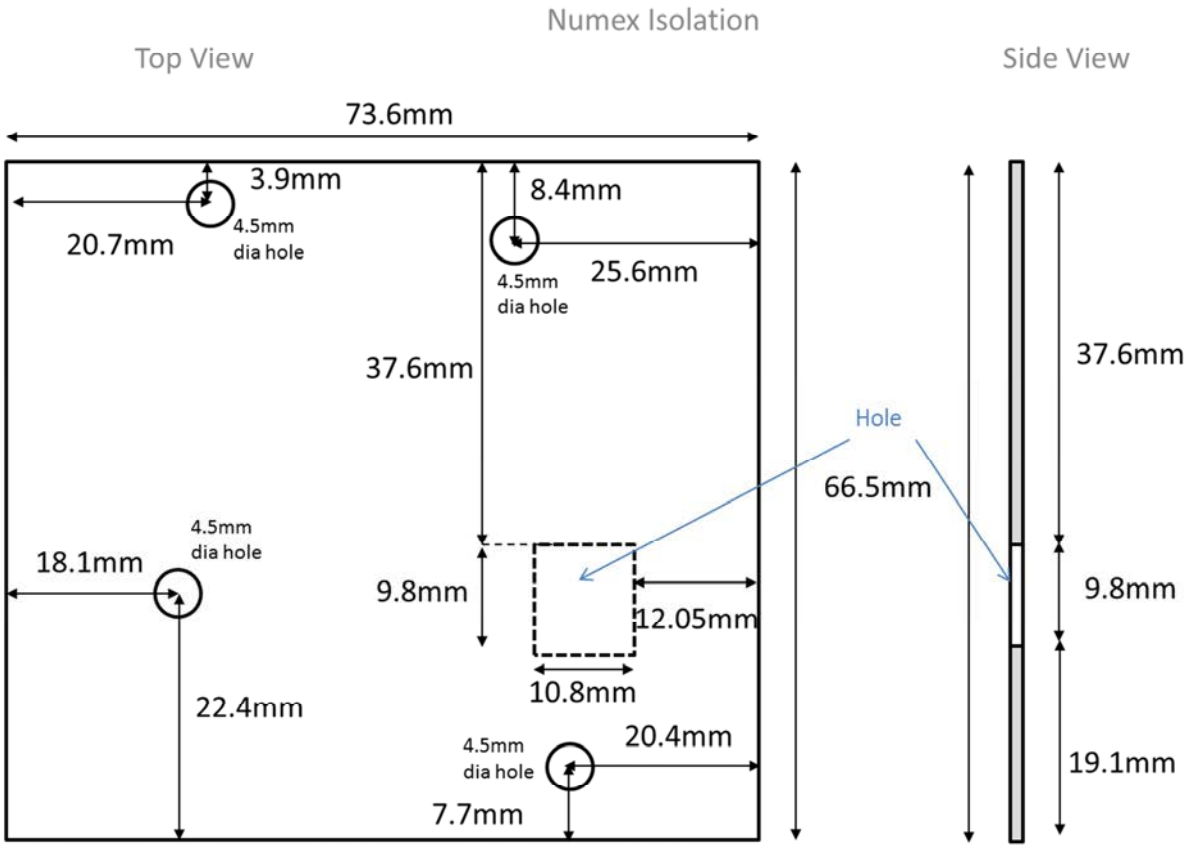


Figure 68 – Isolation Dimensions.

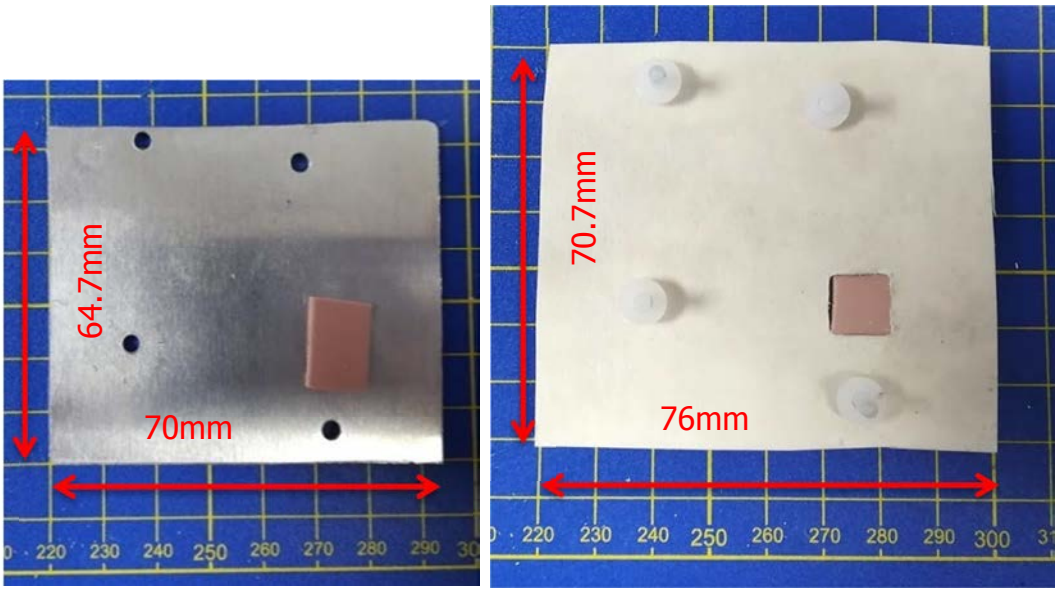


Figure 69 – Heat Sink Aluminum Plate.

Last stage is to assembly the board to the heat sink.

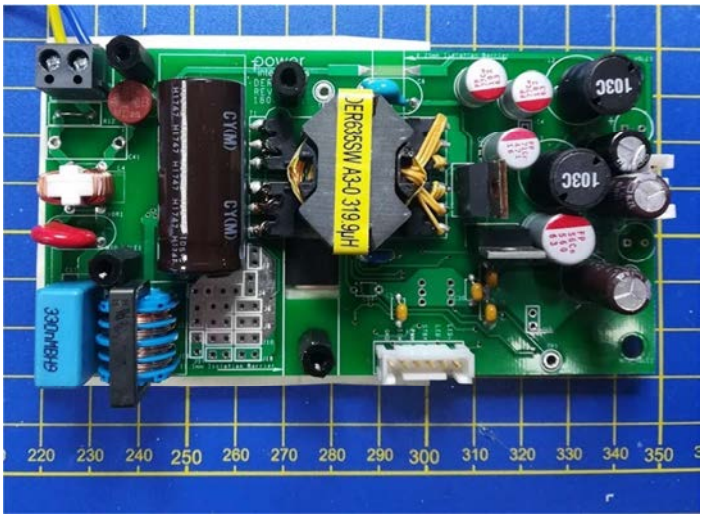


Figure 70 – Cooling Assembly.

16.2 *Thermal Set-Up*

This is the Top view from the thermal camera point of view.

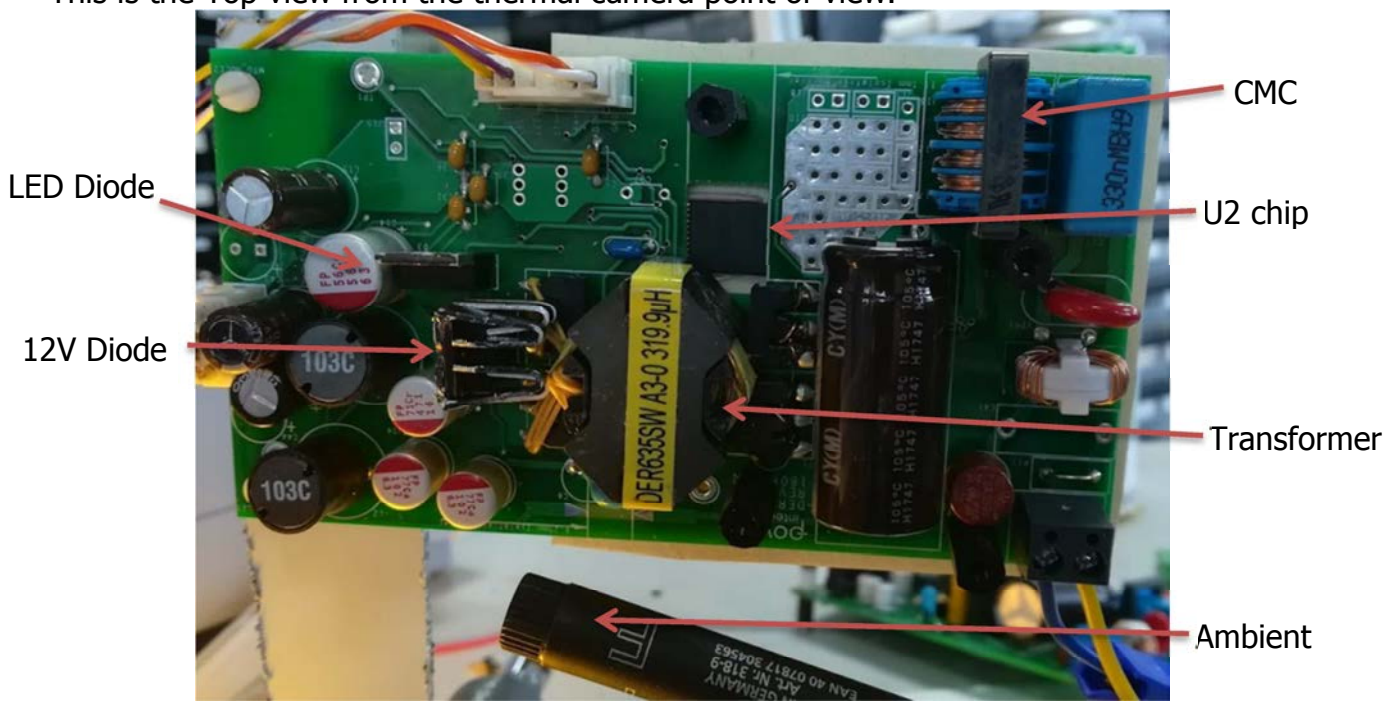


Figure 71 – Top Thermal Set-Up.

This is the Bottom view from the thermal camera point of view.

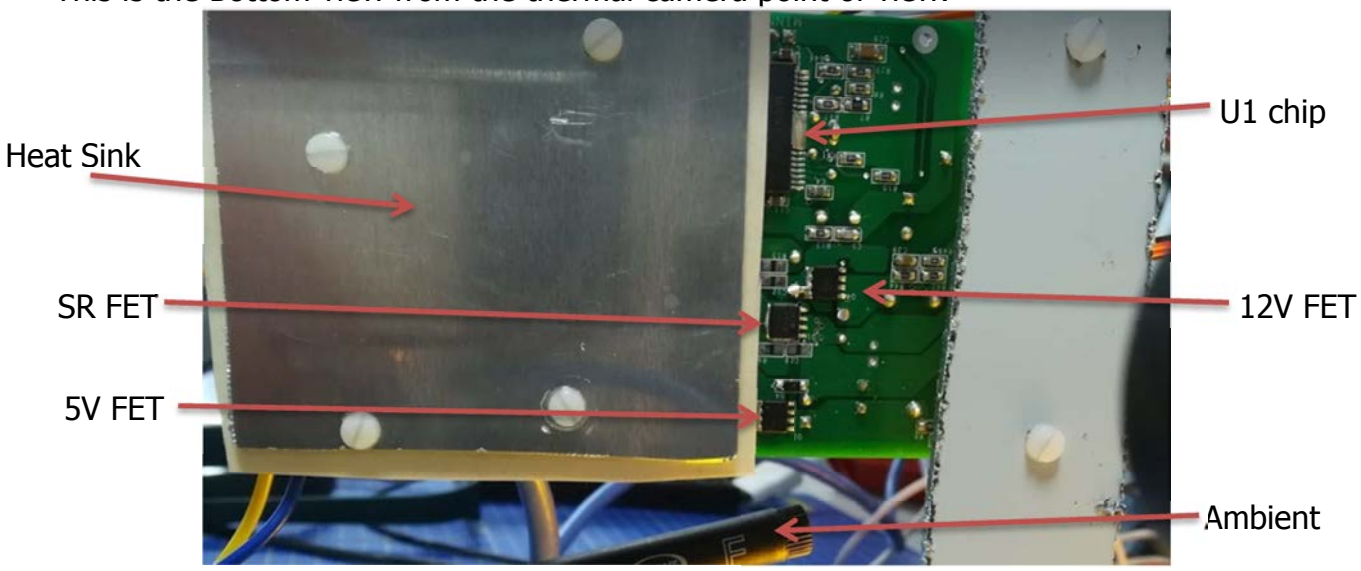


Figure 72 – Bottom Thermal Set-up.

16.3 *90 VAC*

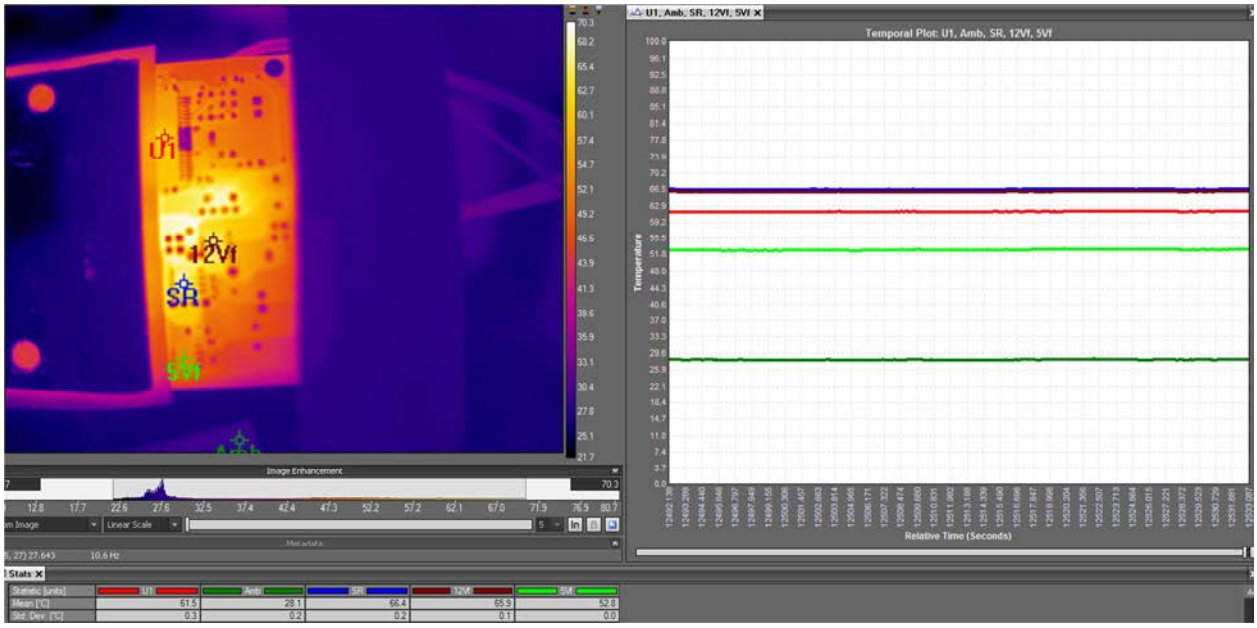


Figure 73 – Line = 90 V Full Power Thermal Image - Bottom View.

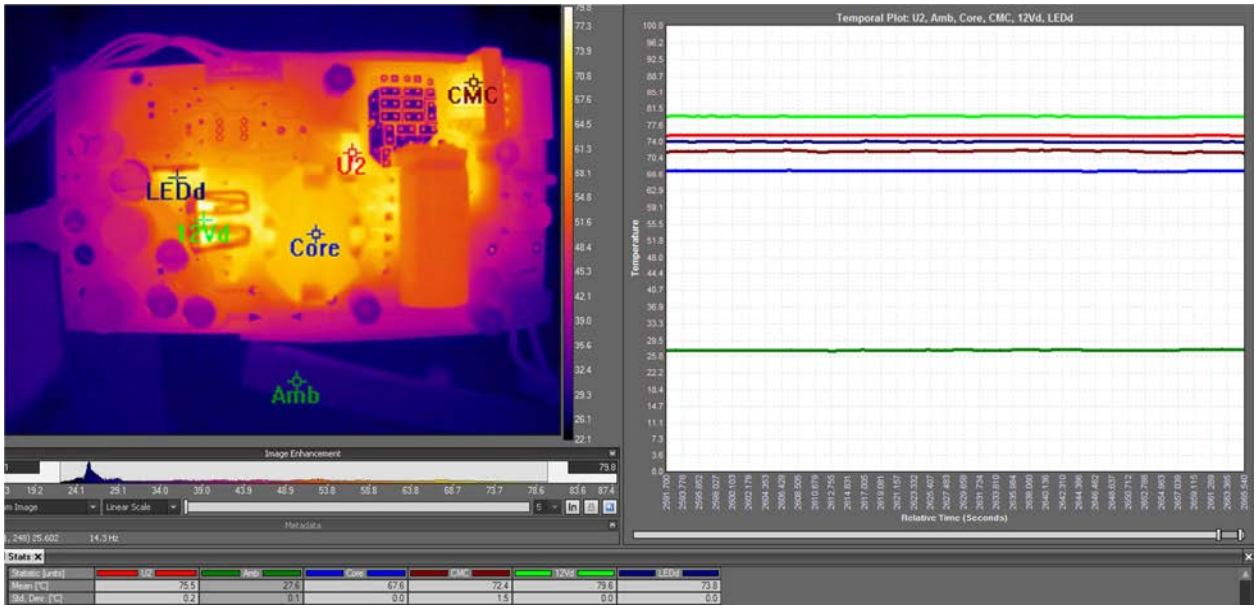


Figure 74 – Line = 90 V Full Power - Thermal Image - Top View.

Part	U2 chip	Core	CMC	12 V Diode	LED Diode	SR FET	5 V FET	12 V FET	U1 chip
T [C°]	75.5	67.6	72.4	79.6	73.8	66.4	52.8	65.9	61.5
ΔT [C°]	47.9	40.4	44.4	52.4	46.4	38.3	24.7	37.8	33.4

Table 17 – Line = 90 V Full Power – Component Temperatures .

16.4 *115 VAC*

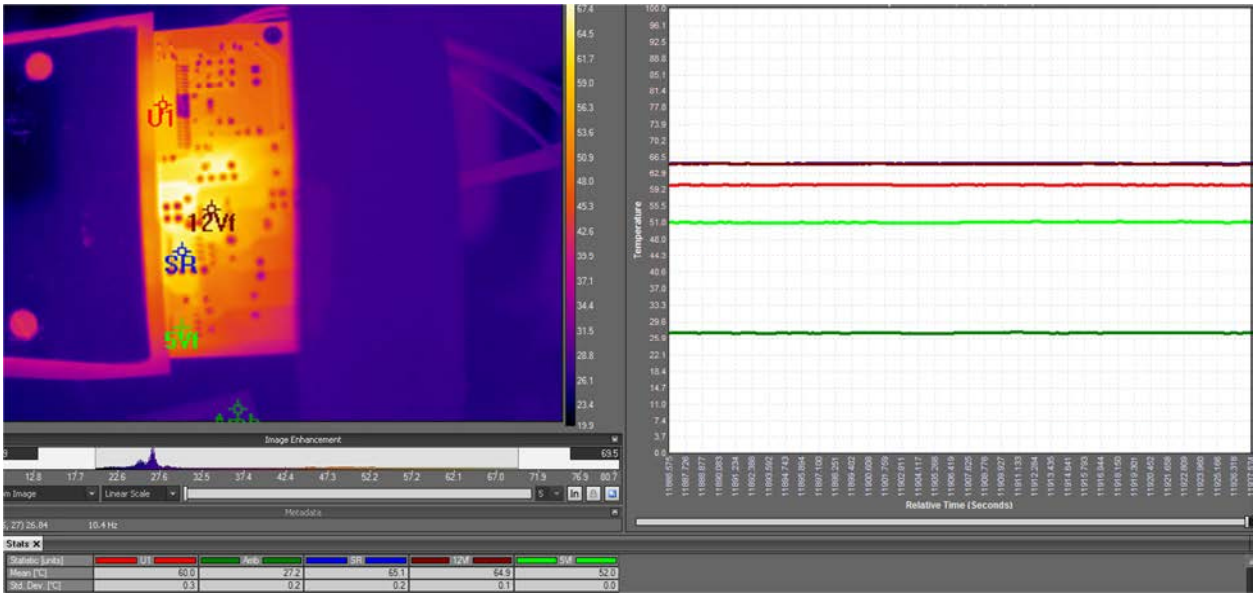


Figure 75 – Line = 115 V Full Power Thermal Image – Bottom View.

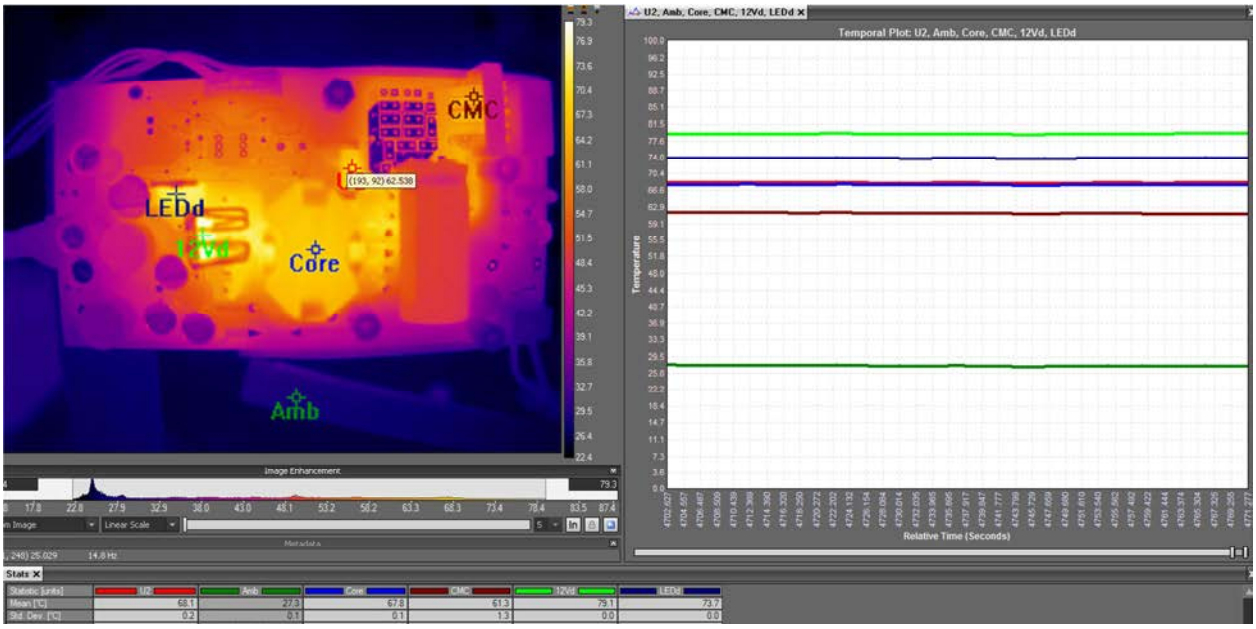


Figure 76 – Line = 115 V Full Power Thermal Image - Top View.

Part	U2 chip	Core	CMC	12 V Diode	LED Diode	SR FET	5 V FET	12 V FET	U1 chip
T [C°]	68.1	67.8	61.3	79.1	73.7	65.1	52	64.9	60
ΔT [C°]	40.8	40.5	34	51.8	46.4	37.9	24.8	37.7	32.8

Table 18 – Line = 115 V Full Power Component Temperatures.

16.5 *230 VAC*

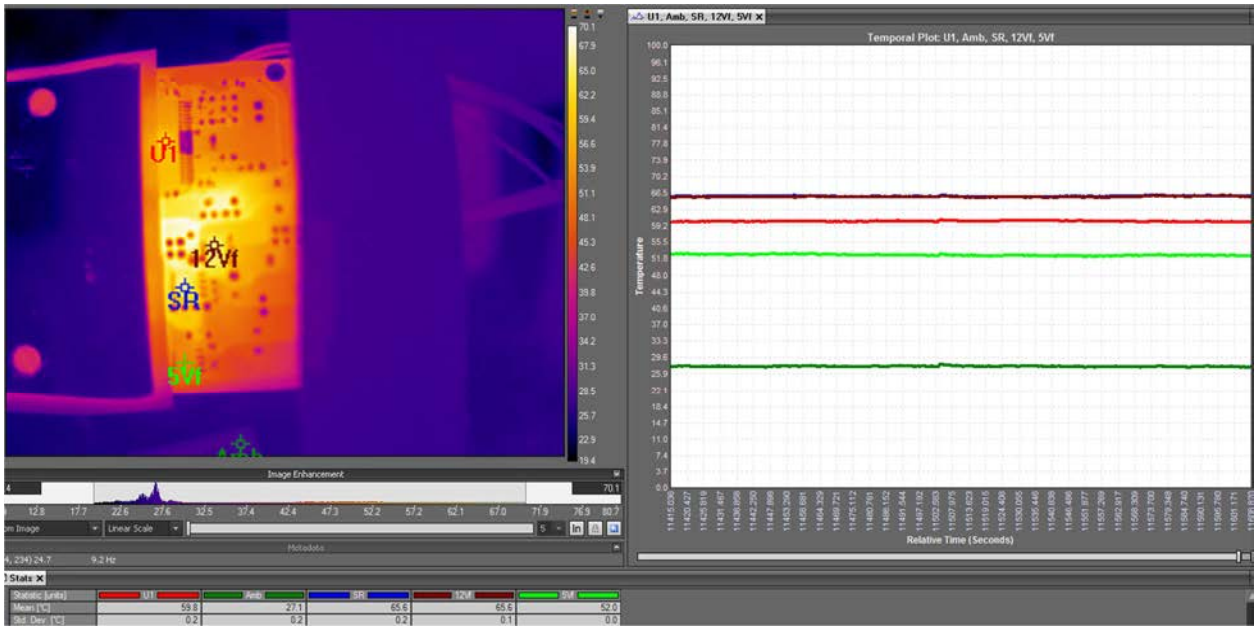


Figure 77 – Line = 230 V Full Power Thermal Image - Bottom View.

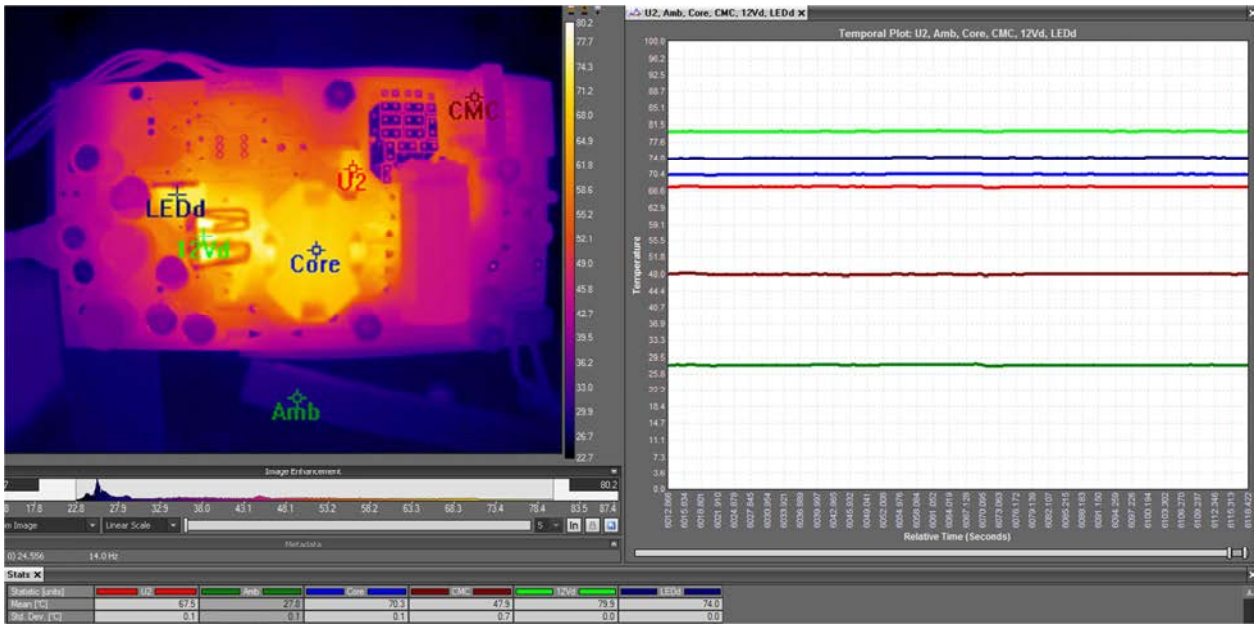


Figure 78 – 230 V Thermal Top View.

Part	U2 chip	Core	CMC	12 V Diode	LED Diode	SR FET	5 V FET	12 V FET	U1 chip
T [C°]	67.5	70.3	47.9	79.9	74	65.6	52	65.6	59.8
ΔT [C°]	39.7	42.5	20.1	52.1	46.2	38.5	24.9	38.5	32.7

Table 19 – Line = 230 V Full Power – Component Temperatures.

16.6 *265 VAC*

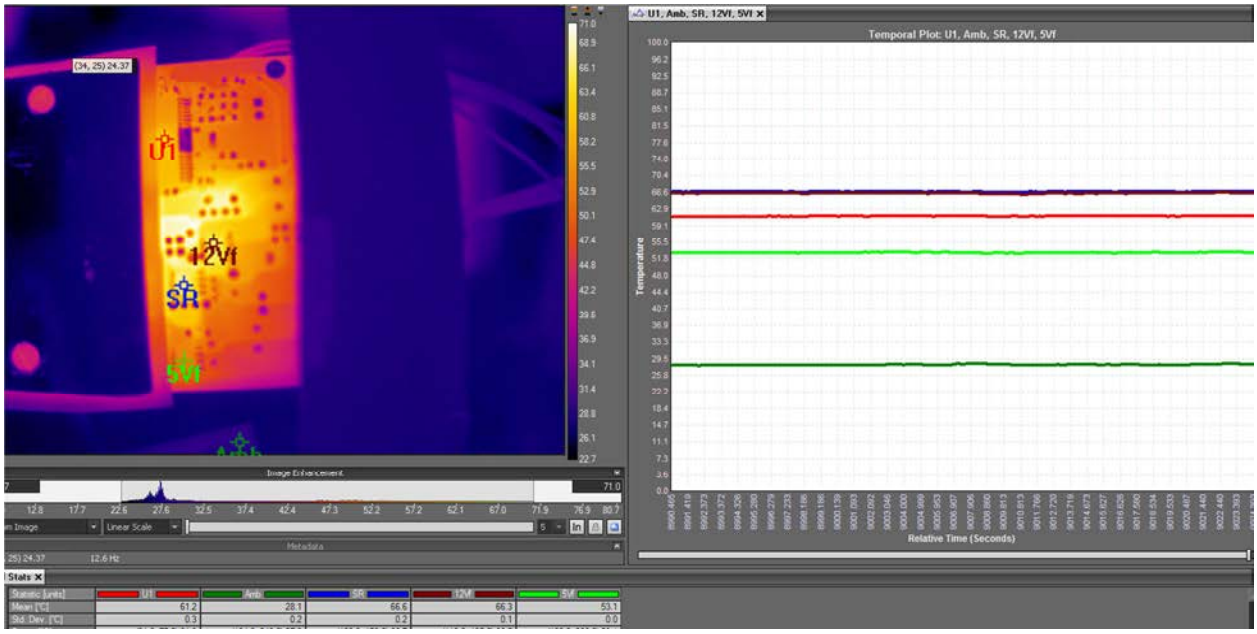


Figure 79 – Line = 265 V Full Power Thermal Image - Bottom View.

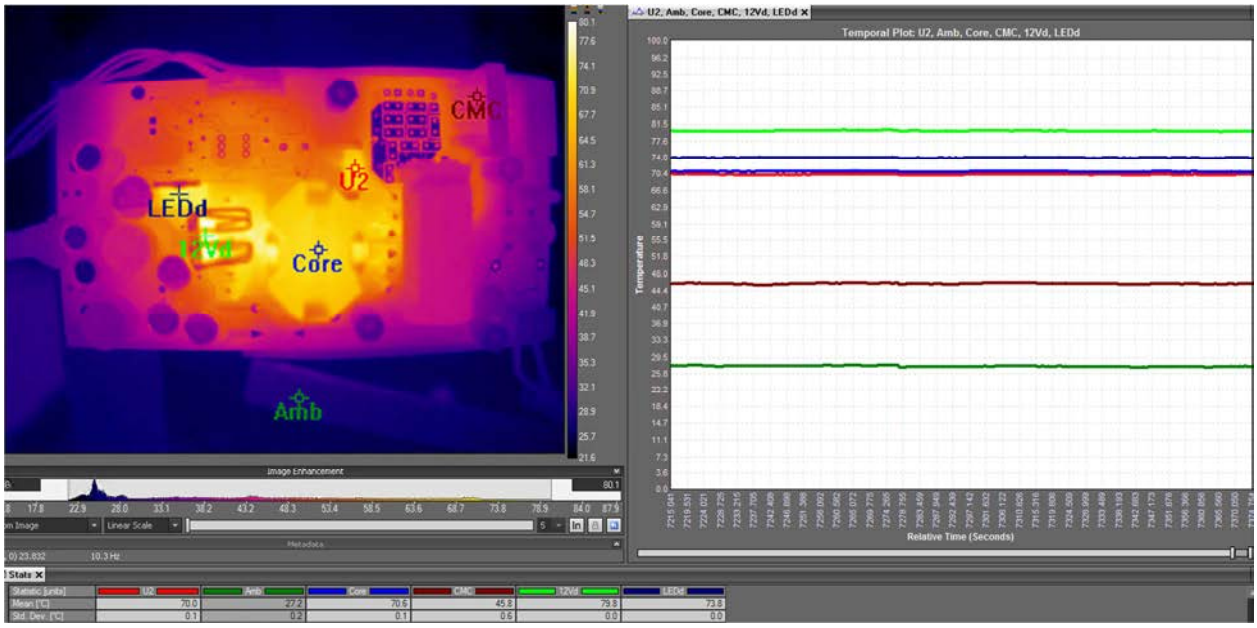


Figure 80 – Line = 265 V Thermal Image - Top View.

Part	U2 chip	Core	CMC	12 V Diode	LED Diode	SR FET	5 V FET	12 V FET	U1 chip
T [C°]	70	70.6	45.8	79.8	73.8	66.6	53.1	66.3	61.2
ΔT [C°]	42.8	43.4	18.6	52.6	46.6	38.5	25	38.2	33.1

Table 20 – Line = 265 V Full Power – Component Temperatures.

17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
5-Mar-19	NE	2.0	Initial Release.	Apps & Mktg
19-Mar-19	EO	3.0	Update for Code L.	Apps & Mktg
21-Aug-19	NE	3.1	Updated Figures 12, 13, 14.	Apps & Mktg
12-Aug-21	KM	3.2	Updated Text and Schematic	Apps & Mktg

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