

Design Example Report

Title	3-Phase Inverter Using BridgeSwitch [™] BRD1165C and LinkSwitch [™] -TN2 LNK3204D with Toshiba TMP375FSDMG Vector Engine Microcontroller (VEMCU) in FOC Operation		
Specification	340 VDC Input, 300 W Three Phase Inverter Output Power, 0.9 A_{RMS} Motor Phase Current (Phase U/V/W), 5000 RPM for 4-Pole Brushless Sensorless Motors		
Application	High-Voltage Brushless DC (BLDC) Motor Drive		
Author	Applications Engineering Department		
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Summary and Features

- BridgeSwitch high-voltage half-bridge motor driver
- Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- No heat sink
- Fully self-biased operation simplifies auxiliary power supply
- High-side and low-side cycle-by-cycle current limit
- Two level device over-temperature protection
- High-voltage bus monitor with four undervoltage threshold and one overvoltage threshold
- System level temperature monitor
- Single wire status update communication bus
- Sensorless field oriented control (FOC)

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Important Note:

During operation, the design example board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.



1 Introduction

This document describes a 300 W, 97% efficient, 3-phase inverter for high-voltage brushless DC (BLDC) motor application using BridgeSwitch BRD1165C device. The design shows the device performance, internal level monitoring, system level monitoring, and fault protection facilitated by the high level of integration of the BridgeSwitch half-bridge motor driver IC. A high-voltage, low component count buck converter employing a LinkSwitch-TN2 LNK3204D device supplies the motor control microcontroller, current sense amplifier, ground sense comparator, UART (Universal Asynchronous Receiver-Transmitter), as well as all logic and interface circuitry.

The Toshiba TMP375FSDMG microcontroller (MCU) is used in this demonstration board design. It is a high-performance microcontroller and incorporates routine processing hardware called "Vector Engine" for motor vector control.

In addition, this document also contains the inverter specification, schematic, bill of materials, printed circuit board (PCB) layout, performance data, and test setup. The provided waveforms along with the design performance are based on a sensorless field oriented control (FOC) motor control method using Toshiba's 32-bit RISC microcontroller TMPM375FSDMG.



Figure 1 – Populated Circuit Board Top View.



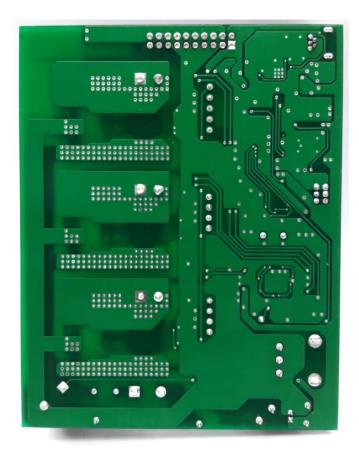


Figure 2 – Populated Circuit Board Bottom View.



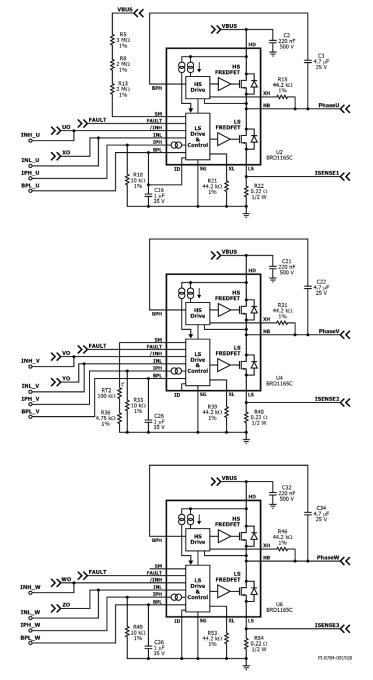
2 Inverter Specification

The table below provides the electrical specification of the 3-phase inverter design. The result section provides actual performance data.

Description	Symbol	Min	Тур	Max	Unit	Comment	
Input							
Voltage	V _{IN}	270	340	365	V	2-wire DC input	
Current	I_{IN}		0.9		A _{RMS}	RMS	
Power	P _{IN}		309		W	At efficiency=97%	
Output							
Power	P _{OUT}		300		W	Inverter output power	
Motor Phase Current	I _{MOTOR}		0.9		A _{RMS}	RMS per phase	
PWM Carrier Frequency ¹	f _{PWM}		12	20	kHz	Self-supplied operation	
Efficiency	n		97		%	RPM= 5000	
Environmental Ambient Temperature	T _{AMB}	0		40	°C	Free convection	
System Level Monitoring DC Bus Sensing OV Threshold 1 st UV Threshold 2 nd UV Threshold 3 rd UV Threshold	V _{OV} V _{UV100} V _{UV85} V _{UV60}		422 247 212 177		V V V V	Reported through Status Communication Bus (fault pin)	
4 th UV Threshold	V _{UV55}		142		V		
Over Current Protection ²	I _{OCP}		3		A _{PK}	At XL/XH = 44.2 kΩ	
System Warning Temperature ³	T _{SYS}		90		°C		
 Notes: 1. 20 kHz is the maximum recommended PWM frequency with self-supply or with external supply. 2. Can be manually configured depending on the value of XL/XH. For BRD1165C the maximum current protection level is 3A at XL/XH=44.2 kΩ. 3. Sensed through an external thermistor, temperature threshold depends on chosen NTC and its location, requires verification in final application. 							
Table 1 – Inverter Specification.							

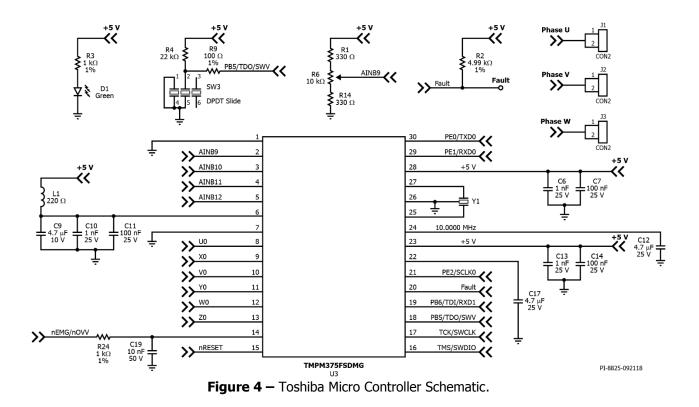


3 Schematic

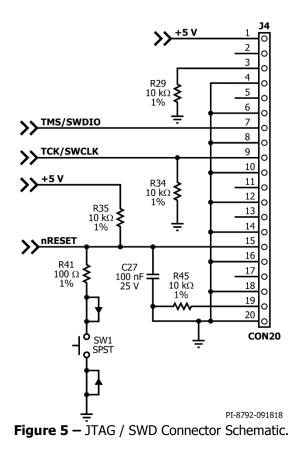












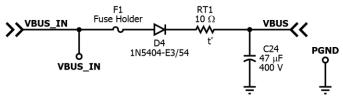


Figure 6 – Bulk Input Circuit Schematic.



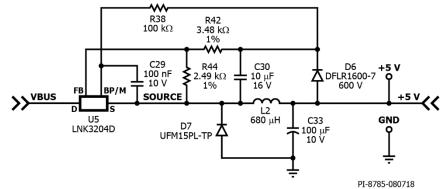
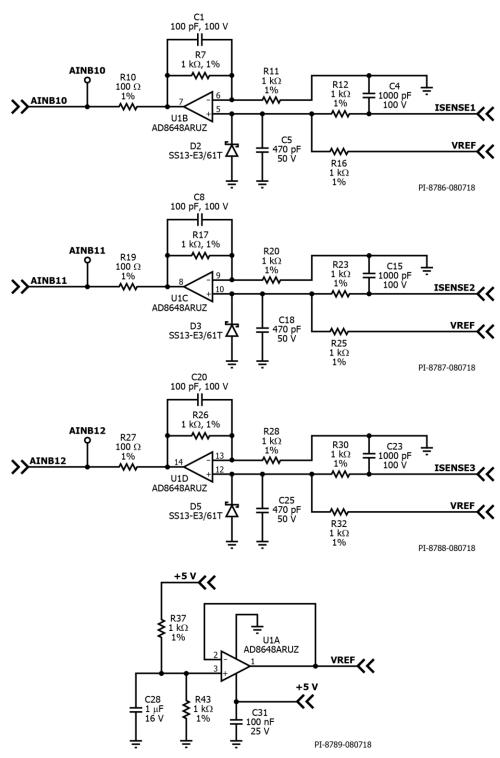


Figure 7 – Auxiliary Circuit Schematic.









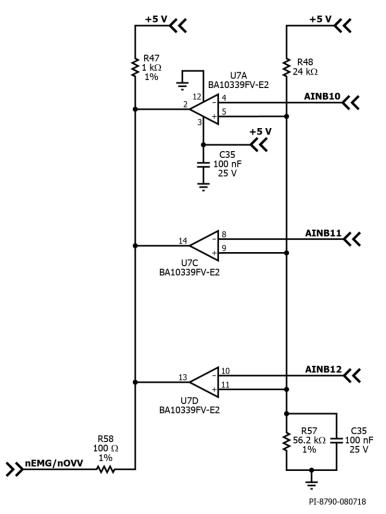


Figure 9 – Ground Sense Comparator Circuit Schematic.

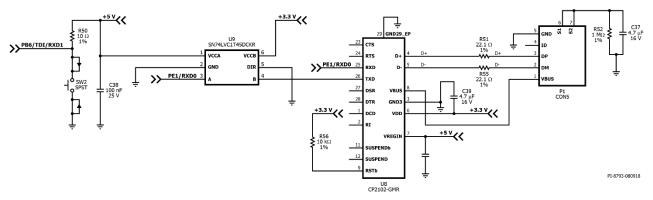


Figure 10 – UART Circuit Schematic.



4 Circuit Description

The overall schematic shows a 3-phase inverter utilizing three BridgeSwitch BRD1165C device. The circuit design drives a high-voltage, 3-phase, brushless DC (BLDC) motor utilizing field oriented control (FOC) for controlling the motor. BridgeSwitch combines two 600 V, N-channel power FREDFETs with its corresponding gate drivers into a low profile surface mount package. The BridgeSwitch power FREDFET features ultra-soft, fast recovery diode ideally suited for inverter drives. Both drivers are fully self-supplied eliminating the need for the system power supply to provide gate drive power.

A LinkSwitch-TN2 LNK3204D device in a high-voltage buck converter provides the supply voltage for the motor control microcontroller TMPM375 from Toshiba and associated circuitry.

In addition, BridgeSwitch incorporates internal fault protection and system level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and a two level thermal overload protection. On the other hand, system level monitoring includes high-voltage DC bus sensing with multi-level under-voltage thresholds and one over-voltage threshold. BridgeSwitch can also be configured using external sensors such as a thermistor for system temperature monitoring. A single wire open Drain bus communicates all detected fault or change of status to the system micro-controller.

4.1 **Three phase BridgeSwitch Inverter**

The three BridgeSwitch devices U2, U4, and U6 form the 3-phase inverter. The output of the inverter connects to the 3-phase BLDC motor through connectors J1, J2, and J3 (Phase U,V,W respectiviely).

4.2 Input Stage

The input stage consist of fuse F1, rectifier diode D4, inrush thermistor RT1, and input capacitor C24. Fuse F1 provides protection when there is an excessive input current. Diode D4 is use for input rectification and circuit protection in case the polarity of the input bus voltage is reverse. Thermistor RT1 is a negative temperature coefficient (NTC) device that initially presents high resistance, which prevents large currents from flowing at turn-on therefore limiting inrush-current. A bulk capacitor C24 is used for high input bus voltage.

4.3 **High-Voltage DC Bus Decoupling Capacitor**

Capacitors C2, C21, and C32 are high voltage capacitors that provide local high frequency decoupling of the DC bus voltage for each BridgeSwitch. The capacitors are physically placed between the BridgeSwitch high DC input voltage pin and the power ground taking into account the required creepage and clearance for the PCB layout.



4.4 Bias Supply

Capacitors C16, C26, and C36 provide self-supply decoupling for the integrated low-side controller and gate driver. Internal high-voltage current source recharges such capacitors as soon as the voltage level starts to dip. On the other hand, capacitors C3, C22, and C34 provide self-supply decoupling for the integrated high-side controller and gate driver. Internal high-voltage current sources recharge these capacitors whenever the half-bridge point of the respective device drops to the low-side source voltage level (i.e. the low-side FREDFET turns on).

4.5 **PWM Input**

Input PWM signals U0, X0, V0, Y0, W0, and Z0 control the switching state of the integrated high side and low side power FREDFETs. The system microcontroller provides the required PWM signal and desired switching frequency.

4.6 Cycle-by-Cycle Current Limit

Resistors R15, R21, R31, R39, R46, and R53 set the cycle-by-cycle current limit level for the integrated low side and high-side power FREDFETs. A selected value of 44.2 k Ω set the current limit to 100% of the default level or 3 A.

4.7 System Underoltage (UV) and Overvoltage (OV) Protection

BridgeSwitch U2 monitors the DC bus voltage through resistors R5 (3 M Ω), R8 (2 M Ω), and R13 (2 M Ω) value. The combined resistance of 7 M Ω sets the under-voltage thresholds to 247 V, 212 V, 177 V, and 142 V. The bus over-voltage threshold is at 422 V. The FAULT-pin reports any detected bus voltage fault condition to the system microcontroller (MCU).

4.8 **System Level Temperature and Monitoring**

BridgeSwitch U4 monitors the system temperature through thermistor RT2 connected to the SM pin. Resistor R36 tunes the threshold for a system level fault of 90 °C. The device reports a detected status change of the externally set system level temperature to the MCU through its FAULT bus.

4.9 **Fault Communication**

The BridgeSwitch device (U2, U4, and U6) reports any detected internal and system status change through the communication bus connected to pin 20 of the microcontroller. The microcontroller takes action in accordance to the status update reported by the device. Such action could be for instance inverter shutdown, latch, restart, warning, etc.

4.10 **Device ID**

Each BRD1165C assigns itself a unique device ID through the connection of pin 11 (ID pin). The pin connection can either be floating, connected to the SG pin or BPL pin.



Device ID enables communicating the actual device flagging a fault to the system microcontroller.

4.11 Microcontroller

Device U3, Toshiba TMP375FSDMG is the microcontroller (MCU) responsible for the overall motor control particularly catering the algorithm for field-oriented control (FOC). In order to facilitate precisely the motor rotation and positioning, current information on each phase coming from sense resistors R22, R40, and R54 passes through current sense amplifier U1B, U1C, and U1D. The information is then directly being fed to pins 3, 4, and 5 (AINB10, AINB11, and AINB12 respectively) of the microcontroller device U3. For more information about Toshiba TMP375FSDMG please refer to the datasheet through the following link:

https://toshiba.semicon-storage.com/us/product/microcomputer/tx03series/detail.TMPM375FSDMG.html

4.12 Current Sense Amplifier

Components U1B, U1C, and U1D are current sense amplifiers, which gathers data from sense resistors R22, R40, and R54. The current information from these sense resistors are being offset to 2.5 VDC level in the op-amp output pins. U1A circuit provides the 2.5 VDC offset reference voltage. The current information from the output of U1B, U1C, and U1C passes to the microcontroller that modulates the PWM input to the BridgeSwitch inverter maintaining desired power and RPM.

Note: U1A, U1B, U1C, and U1D are op-amps in one IC package (Quad op-amp, U1)

4.13 Ground Sense Comparator Circuit

Device U7A, U7C, and U7D is a ground comparator circuit that turns off the PWM whenever an excessive current is detected through the current sense amplifier U1. The output voltage of the current sense amplifier circuit AINB10, AINB11, and AINB12 is constantly compared to a voltage divider voltage value on R48 and R57. The output of the comparator circuit is tied directly to the microcontroller such that if it goes low, the PWM be inhibited.

Note: U7A, U7C, and U7D are comparators in one IC package (Quad comparator, U7)

4.14 Auxiliary Power Supply Circuit

Device U5 (LNK3204D) is a high side buck switcher IC responsible for providing 5 V supply to the microcontroller, interface circuits, and current sense amplifier circuitry. It directly steps down the high input DC voltage to the desired low output voltage. For more information about LNK3204D, please refer to the datasheet through the following link:

https://ac-dc.power.com/design-support/product-documents/data-sheets/linkswitch-tn2data-sheet/



4.15 **Motor Connector**

Connectors J1, J2, and J3 (Phase U, V, and W respectively) are mechanical connectors that directly connect the BridgeSwitch 3-phase inverter to the BLDC motor.

4.16 JTAG/SWD Connector

Device J4 is the JTAG connector interface for the programming device and the microcontroller. For more information about programming device, please refer to the following link:

https://store.iar.com/product/I-jet

4.17 UART Circuit

Device U8 is a UART (Universal Asynchronous Receiver-Transmitter) device responsible for facilitating the fault communication between the microcontroller and a computing device (computer, laptop, PC) through data communications interface / connector P1.



5 Printed Circuit Board Layout

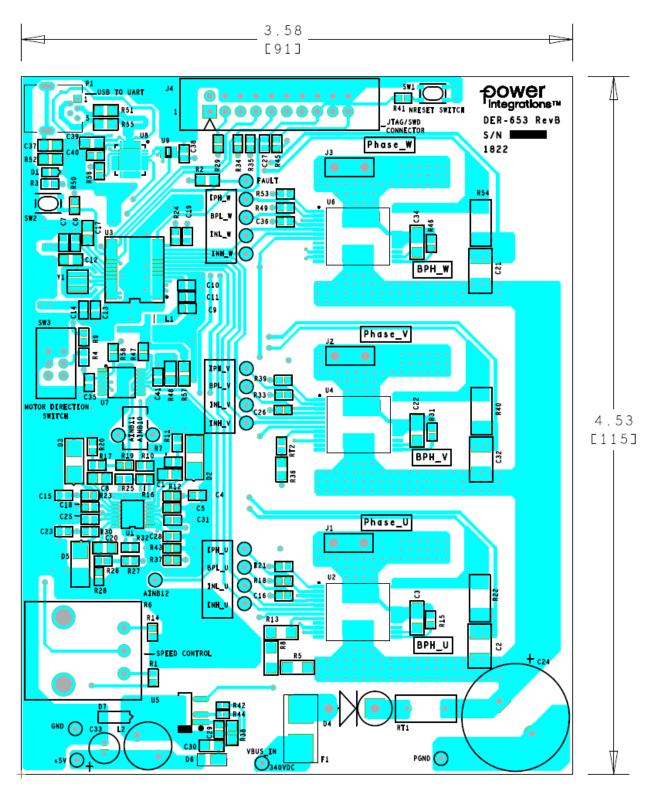


Figure 11 – Printed Circuit Board Layout Top View.





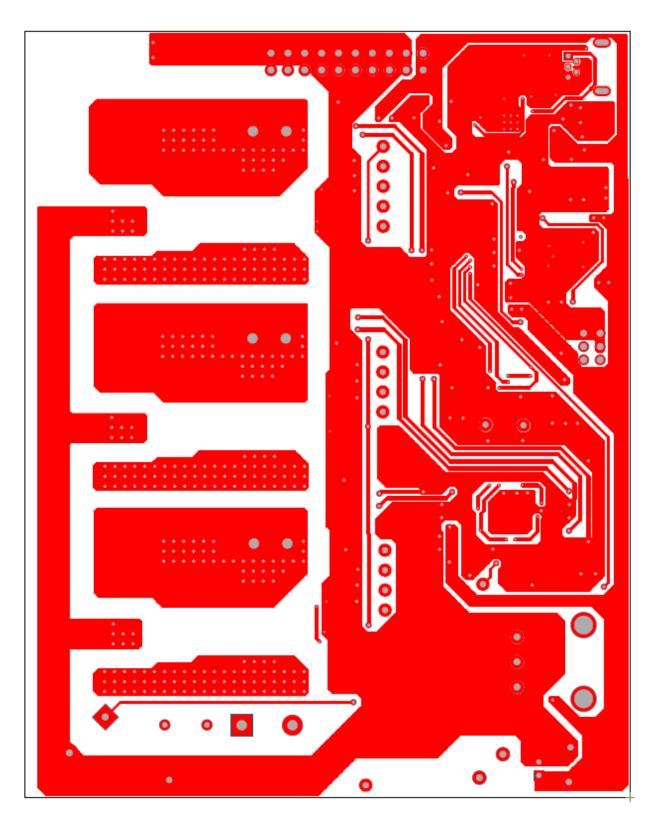


Figure 12 – Printed Circuit Board Layout Bottom View.





6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	20	+5V,AINB10,AINB11,AINB12, BPL_U,BPL_V,BPL_W, FAULT,GND, INH_U,INH_V,INH_W, INL_U,INL_V,INL_W, IPH_U,IPH_V,IPH_W, PGND,VBUS_IN	CONN, PC, PIN, CIRC, 0.030" (0.76 mm) Dia, GOLD	6821-0-00-15-00-00-08-0	Mill-Max Mfg
2	3	C1,C8,C20	100 pF, 100 V, Ceramic, COG, 0805	C0805C101J1GACTU	Kemet
3	3	C2,C21,C32	220 nF, 500 V, Ceramic, X7R, 1812	C1812C224KCRACTU	Kemet
4	3	C3,C22,C34	4.7 μF, ±10%, 25 V, Ceramic, X7R, 1206	GCM31CR71E475KA55L	Murata
5	3	C4,C15,C23	1000 pF, 100 V, Ceramic, NP0, 0603	C1608C0G2A102J	TDK
6	3	C5,C18,C25	470 pF 50 V, Ceramic, X7R, 0603	C1608C0G1H471J080AA VJ0603A471JXAAC	TDK Vishay
7	3	C6,C10,C13	1 nF, 25 V, Ceramic, X7R, 0603	GRM188R71E102KA01D GCM188R71E102KA37D	Murata
8	7	C7,C11,C14, C27,C31,C35,C38	100 nF, 25 V, Ceramic, X7R, Epoxy Mountable, Non- Magnetic, 0603	VJ0603Y104KNXAO	Vishay
9	1	С9	4.7 μF, 10 V, Ceramic, X5R, 0603	C1608X5R1A475M/0.50	TDK
10	4	C12,C17,C37,C39	4.7 μF, ±10%, 25 V, Ceramic, X7R, -55°C ~ 125°C, 0805 ΤΜΚ212ΑΒ7475ΚG		Taiyo Yuden
11	3	C16,C26,C36	1 μF, ±10%,35 V, Ceramic, X7R, AEC-Q200, Automotive, 0603	CGA3E1X7R1 V105K080AC	TDK
12	1	C19	10 nF 50 V, Ceramic, X7R, 0603	C0603C103K5RACTU	Kemet
13	1	C24	47 μF, 400 V, Electrolytic, Low ESR, 750 mΩ, (18 x 20)	EKMX401ELL470MM20S	Nippon Chemi-Con
14	3	C28,C40,C41	1 μF 16 V, Ceramic, X7R, 0603 C1608X7R1C10 CL10B105K08VF		TDK Samsung
15	1	C29	100 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H104K GCM188R71H104KA57J	TDK Murata
16	1	C30	10 μF, ±10%, 16V, X7R, Ceramic Capacitor, Surface Mount, MLCC 0805 (2012 Metric)	CL21B106KOQNNNE	Samsung
17	1	C33	100 μ F, 10 V, Electrolytic, Low ESR, 500 m Ω , (5 x 11.5)	ELXZ100ELL101MEB5D	Nippon Chemi-Con
18	1	D1	LED, GREEN, 525 nm, 3.2 V, 20 mA, 260.5mcd, RECT, CLEAR, 0603	LTST-C194TGKT	Lite-On
19	3	D2,D3,D5	30 V, 1 A, Schottky, SMD, DO- 214AC	SS13-E3/61T	Vishay
20	1	D4	400 V, 3 A, Recitifier, DO- 201AD	1N5404-E3/54	Vishay
21	1	D6	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
22	1	D7	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123		Micro Commercial
23	1	F1	HOLDER, FUSE, BLOCK, CARTRIDGE, 125 V 10 A, SMD	01550900M	Little Fuse
24	3	J1,J2,J3	CONN QC TAB 0.250 SOLDER	1287-ST	KeyStone
25	1]4	20 Pos (2 x 10), Female,Shrouded, header, HIF3FC-20PA-2.54DSA(71)		Hirose Electric



			0.100" (2.54 mm)		1
			pitch,Straight, low profile, Gold, Through Hole		
26	1	L1	FERRITE BEAD, 220 Ω, 2A, 0805, 1LN, 45 mΩ	BLM21PG221SN1D	Murata
27	1	L2	680 μH, 0.36 A	SBC3-681-361	SUNX
28	1	P1	USB, mini B Recpt, Conn, 5 Pos, TH, Right Angle, Horizontal	1734510-1	TE/AMP Connectors
29	2	R1,R14	RES, 330 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ331 V	Panasonic
30	1	R2	RES, 4.99 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4991 V	Panasonic
31	17	R3,R7,R11,R12, R16,R17,R20,R23, R24,R25,R26,R28, R30,R32,R37,R43,R47	RES, 1 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1001 V	Panasonic
32	1	R4	RES, 22 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ223V	Panasonic
33	1	R5	RES, 3 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF3004	Rohm Semi
34	1	R6	POT, 10 kΩ, 20%, 1/8 W, Vertical	296UD103B1N	CTS.
35	2	R8,R13	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004 V	Panasonic
36	6	R9,R10,R19, R27,R41,R58	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
37	6	R15,R21,R31, R39,R46,R53	RES, 44.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4422 V	Panasonic
38	8	R18,R29,R33,R34, R35,R45,R49,R56	RES, 10 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1002 V	Panasonic
39	3	R22,R40,R54	RES, 0.22 Ω, 5%, 1/2 W, Thick Film, 2010	ERJ14RQJR22 V	Panasonic
40	1	R36	RES, 4.75 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4751 V	Panasonic
41	1	R38	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104 V	Panasonic
42	1	R42	RES, 3.48 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3481X	Panasonic
43	1	R44	RES, 2.49 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2491X	Panasonic
44	1	R48	RES, 24 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ243V	Panasonic
45	1	R50	RES, 10 Ω, 1%, 1/16 W, Thick Film, 0603 RES, 22.1 Ω, 1%, 1/8 W,	ERJ-3EKF10R0V	Panasonic
46	2	R51,R55	Thick Film, 0805	ERJ-6ENF22R1 V	Panasonic
47	1	R52	RES, 1 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1004 V	Panasonic
48 49	1	R57	RES, 56.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5622 V	Panasonic
	1	RT1	NTC Thermistor, 10 Ω , 1.7 A NTC Thermistor, 100 k Ω , 3%,	CL-120	Thermometrics
50	1	RT2	0603	NCP18WF104E03RB	Murata
51	2	SW1,SW2	SWITCH, TACTILE, SPST-NO, 0.02 A, 15 V, 4.2x3.2x2.5 mm, 160gf, BLACK button	SKRPABE010	ALPS
52	1	SW3	Slide Switch, DPDT, Through Hole	EG2209	E-Switch
53	1	U1	IC, GP OPAmp, Quad, R2R, 14-TSSOP	AD8648ARUZ-REEL	Analog Devices



DER-653 BridgeSwitch BRD1165C 3-Phase Inverter

54	3	U2,U4,U6	BridgeSwitch, Full Featured, Max. BLDC Motor Current 1.0 A (RMS)	BRD1165C	Power Integrations
55	1	U3	IC, MCU, ARM, 32 bit, RISC, TX03 Series, Microcontrollers	TMPM375FSDMG	Toshiba
56	1	U5	LinkSwitch-TN2, SO-8C	LNK3204D	Power Integrations
57	1	U7	IC, COMPARATOR, QUAD, 18 V, SSOP-B14	BA10339FV-E2	Rohm
58	1	U8	IC, USB Bridge, USB to UART USB 2.0 UART Interface, 28- QFN (5x5)	CP2102-GMR	Silicon Labs
59	1	U9	IC, BUS TRANSCVR, TRI-ST, Voltage Level Translator, Bidirectional, 1 Circuit, 1 Channel, 420 Mbps, SC-70-6, SC70-6	SN74LVC1T45DCKR	Texas Instruments
60	1	Y1	10 MHz Ceramic Resonator, Built in Capacitor, 22pF \pm 0.4%, 30 Ω , -25°C ~ 85°C, SMD	AWSCR-16.00CV-T	Abracon

7 Performance Data

This section presents waveform plots and performance data of the BridgeSwitch inverter. The high voltage (VBUS) level is 340 VDC unless stated otherwise. Light load measurements describe the inverter operating with no mechanical brake load applied to the motor. Full load operation describes the inverter operating 300 W output power (refer to Appendix 8.6 for the details on the method applied to measure output power in a 3-phase inverter).. All measurements were performed at room ambient temperature.

7.1 Start-Up Operation

7.1.1 BPL and BPH Start-Up Waveforms

The waveforms show the low-side and high-side bypass pin voltages of device U6 (Phase W) after VBUS = 340 VDC bus turns on. The start-up power up sequence follows the recommended start-up sequence described in section 8.1. The VBUS turn-on slew rate is set at 5 V / ms.

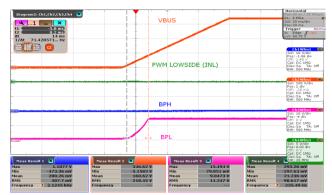


Figure 13 - BPL/BPH Start-up at Light Load, INL = 0 V.CH2: V_{BUS} , 100 V / div.CH4: V_{INL} , 5 V / div.CH1: V_{BPH} , 10 V / div.CH3: V_{BPL} , 10 V / div.Time Scale: 20 ms / div.BPL Rise Time = 14 ms.



 $\label{eq:Figure 14} \begin{array}{l} \textbf{Figure 14} & - \ \text{BPL/BPH Start-up at Light Load, INL} = 5 \ \text{V}. \\ & \ \text{CH2: } V_{\text{BUS}}, \ 100 \ \text{V} \ / \ \text{div}. \\ & \ \text{CH4: } V_{\text{INL}}, \ 5 \ \text{V} \ / \ \text{div}. \\ & \ \text{CH1: } V_{\text{BPH}}, \ 10 \ \text{V} \ / \ \text{div}. \\ & \ \text{CH3: } V_{\text{BPL}}, \ 10 \ \text{V} \ / \ \text{div}. \\ & \ \text{Time Scale: } 20 \ \text{ms} \ / \ \text{div}. \\ & \ \text{BPH Rise Time} = \ 13.21 \ \text{ms}. \end{array}$



7.1.2 *Motor Start-Up Waveforms*

The waveforms below demonstrate the motor start-up of the BridgeSwitch FOC inverter at light load up to 200 W loading condition. VBUS is set at 340 VDC and motor maximum speed is set at 5000 RPM.

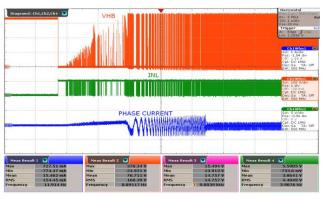


Figure 15 – Motor Start-up at Light Load. CH2: V_{HB} , 100 V / div. CH4: V_{INL} , 5 V / div. CH1: $I_{PHASE_CURRENT}$, 1 A / div. Time Scale: 1 s / div. Maximum Phase Peak Current = 727.51 mA_{PK}. Maximum VHB Peak Voltage = 370.34 V_{PK}.

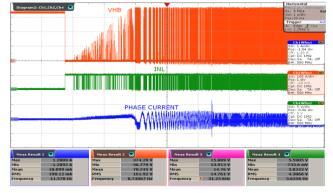


Figure 16 – Motor Start-up at 50 W Load.

CH2: V_{HB} , 100 V / div. CH4: V_{INL} , 5 V / div. CH1: $I_{PHASE_CURRENT}$, 1 A / div. Time Scale: 1 s / div. Maximum Phase Peak Current = 1.28 A_{PK}. Maximum VHB Peak Voltage = 374.29 V_{PK}.

2018-07-05

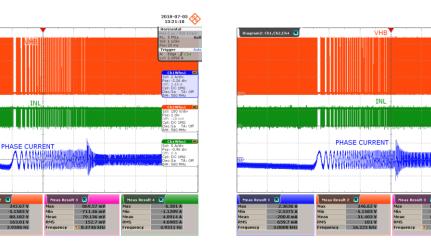


Figure 17 – Motor Start-up at 100 W Load. CH2: V_{HB} , 100 V / div.

CH2: V_{HB} , 100 V / div. CH4: V_{INL} , 5 V / div. CH1: $I_{PHASE_CURRENT}$, 2 A / div. Time Scale: 1 s / div. Maximum Phase Peak Current = 2.52 A_{PK}. Maximum VHB Peak Voltage = 342.67 V_{PK}. Figure 18 – Motor Start-up at 200 W Load.

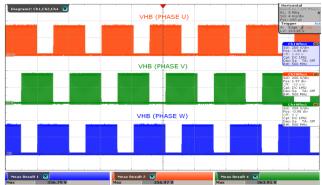
 $\begin{array}{l} \mbox{CH2: V_{HB}, 100 V / div.} \\ \mbox{CH4: V_{INL}, 5 V / div.} \\ \mbox{CH1: $I_{PHASE_CURRENT$, 2 A / div.} \\ \mbox{Time Scale: 1 s / div.} \\ \mbox{Maximum Phase Peak Current} = 2.36 A_{PK}. \\ \mbox{Maximum VHB Peak Voltage} = 346.62 V_{PK}. \end{array}$



7.2 Steady-State Operation

7.2.1 Phase Voltages (Drain to Source) During Steady-State

The waveforms below show the phase voltages of the BridgeSwitch (low side drain to source voltage) 3-phase inverter using field oriented control. Maximum peak voltage was measured from light to full load (inverter load) during steady state operation. VBUS = 340 VDC and the motor speed is 5000 RPM.



 $\label{eq:Figure 19-Drain to Source Voltage at Light Load. \\ CH2: V_{HB_PHASEU, 200 V / div.} \\ CH4: V_{HB_PHASEV, 200 V / div.} \\ CH1: V_{HB_PHASEV, 200 V / div.} \\ Time Scale: 4 ms / div. \\ Maximum Peak Voltage (U) = 356.97 V_{PK}. \\ Maximum Peak Voltage (V) = 363.91 V_{PK}. \\ Maximum Peak Voltage (W) = 356.79 V_{PK}. \\ \end{array}$

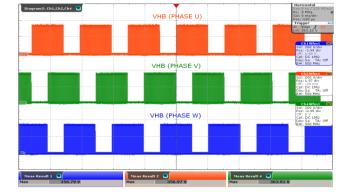
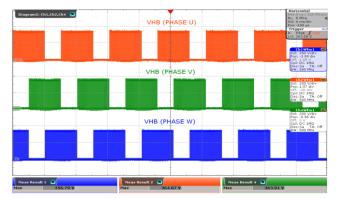
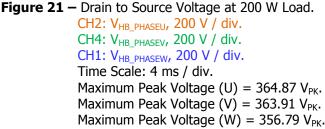


Figure 20 – Drain to Source Voltage at 100 W Load.

CH2: V_{HB_PHASEU} , 200 V / div. CH4: V_{HB_PHASEV} , 200 V / div. CH1: V_{HB_PHASEV} , 200 V / div. Time Scale: 4 ms / div. Maximum Peak Voltage (U) = 356.97 V_{PK}. Maximum Peak Voltage (V) = 363.91 V_{PK}. Maximum Peak Voltage (W) = 356.79 V_{PK}.





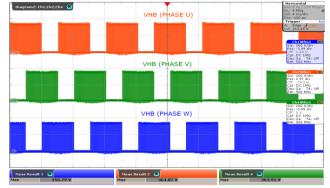


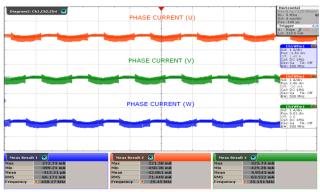
Figure 22 – Drain to Source Voltage at 300 W Load.

CH2: V_{HB_PHASEU} , 200 V / div. CH4: V_{HB_PHASEV} , 200 V / div. CH1: V_{HB_PHASEV} , 200 V / div. Time Scale: 4 ms / div. Maximum Peak Voltage (U) = 364.87 V_{PK}. Maximum Peak Voltage (V) = 363.91 V_{PK}. Maximum Peak Voltage (W) = 356.79 V_{PK}.



7.2.2 Phase Currents During Steady-State

The waveforms below show the phase currents of the BridgeSwitch 3-phase inverter using field oriented method of control (FOC) . Maximum peak current were measured from light load to full load condition during steady state operation.



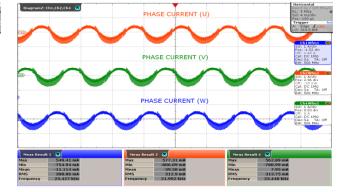


Figure 23 – Phase Current at Light Load. CH2: I_{PHASEU} , 1 A / div. CH4: I_{PHASEV} , 1 A / div. CH1: I_{PHASEW} , 1 A / div. Time Scale: 4 ms / div. RMS Current (U) = 71.44 mA_{RMS}. RMS Current (V) = 63.52 mA_{RMS}. RMS Current (W) = 66.17 mA_{RMS}.



CH2: I_{PHASEU} , 1 A / div. CH4: I_{PHASEV} , 1 A / div. CH1: I_{PHASEV} , 1 A / div. Time Scale: 4 ms / div. RMS Current (U) = 312.90 mA_{RMS}. RMS Current (V) = 313.75 mA_{RMS}. RMS Current (W) = 308.86 mA_{RMS}.

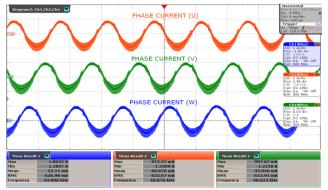
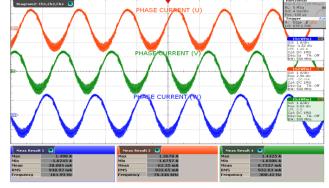


Figure 25 – Phase Current at 200 W Load. CH2: I_{PHASEU} , 1 A / div. CH4: I_{PHASEV} , 1 A / div. CH1: I_{PHASEW} , 1 A / div. Time Scale: 4 ms / div. RMS Current (U) = 625.67 mA_{RMS}. RMS Current (V) = 612.91 mA_{RMS}. RMS Current (W) = 626.98 mA_{RMS}.



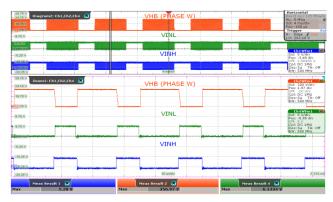


- CH2: I_{PHASEU}, 1 A / div. CH4: I_{PHASEV}, 1 A / div.
- CH1: I_{PHASEW}, 1 A / div.
- Time Scale: 4 ms / div. RMS Current (U) = 933.65 mA_{RMS}.
- RMS Current (V) = 932.63 mA_{RMS}.
- RMS Current $(W) = 938.92 \text{ mA}_{RMS}$.



7.2.3 INL and /INH Signals

The waveforms below show the low-side (INL) and high-side (/INH) input PWM signals during light load and full load condition at steady state operation. PWM frequency is set at 12 kHz with a motor speed of 5000 RPM.





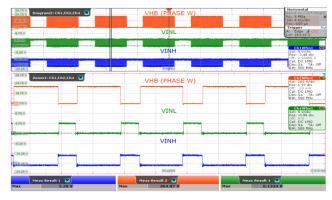


Figure 29 – INL and /INH Signal at 200 W Load. CH2: V_{HB_PHASEW} , 200 V / div. CH4: V_{INL} , 5 V / div. CH1: V_{INH} , 5 V / div. Time Scale: 4 ms / div. Time Scale (Zoomed Area): 20 µs / div.

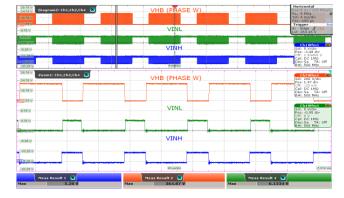


Figure 28 – INL and /INH Signal at 100 W Load.

CH2: V_{HB_PHASEW} , 200 V / div. CH4: V_{INL} , 5 V / div. CH1: V_{INH} , 5 V / div. Time Scale: 4 ms / div. Time Scale (Zoomed Area): 20 µs / div.

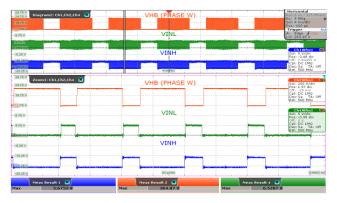


Figure 30 – INL and /INH Signal at 300 W Load. CH2: V_{HB PHASEW}, 200 V / div.

CH2: v_{HB_PHASEW} , 200 V / div. CH4: V_{INL} , 5 V / div. CH1: V_{INH} , 5 V / div. Time Scale: 4 ms / div. Time Scale (Zoomed Area): 20 µs / div.



7.2.4 BPH and BPL during Steady-State

The waveforms below show the BPL and BPH (low-side and high-side self-supply bias level respectively) from light load to full load condition during steady-state operation.

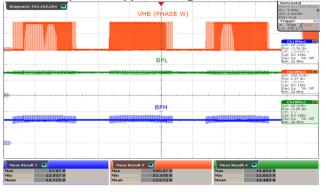


Figure 31 – INL and /INH Signal at Light Load. CH2: V_{HB_PHASEW} , 200 V / div. CH4: V_{BPL} , 10 V / div. CH1: V_{BPH} , 10 V / div. Time Scale: 2 ms / div. BPL Average Voltage = 14.40 V. BPH Average Voltage = 14.72 V.

Diagram2: Ch1,Ch2,Ch4	VHB (PHASE W)		Horizontal Bartians / 250 MSave Rt. 5 MSa Sdi 2 ms/div Pesi - 4 us Trigger Aut A: Edge & Ch2 Lvi: 288.7 V Ch1 W/m1 Sdi 10 V/dy Pesi - 3.76 div
	BPL		Off: 2.50455 V Cpl: DC 1M0 Dec:Sa TA: Off BW: 20 MHz
			Sol: 200 V/div Pos: 1.97 div Off: -20 mV Cpl: DC 1MQ Dec: Sa TA: Off BW: 20 MHz
	BPH	no.diffutuutuutuutuu	Ch4Wfm1 Sol: 10 V/div Pos: -0.95 div Off: 0 V Cpl: DC 1M0 Dec:Sa TA: Off
allish a sensiti fita sensiti f		think out and the second of the	BW: 20 MHz
Meas Result 1	Meas Result 2	Meas Result 4 🐹	
Max 18.365 V Min 12.437 V Mean 14.702 V	Max 356.97 V Min -30,384 V Mean 123.68 V	Max 16.219 Min 12.662 Mean 14.393	V

Figure 33 – INL and /INH Signal at 200 W Load. CH2: V_{HB_PHASEW} , 200 V / div. CH4: V_{BPL} , 10 V / div. CH1: V_{BPH} , 10 V / div. Time Scale: 2 ms / div. BPL Average Voltage = 14.39 V. BPH Average Voltage = 14.70 V.

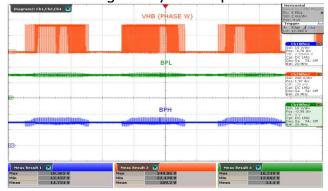


Figure 32 – INL and /INH Signal at 100 W Load. CH2: V_{HB_PHASEW} , 200 V / div. CH4: V_{BPL} , 10 V / div. CH1: V_{BPH} , 10 V / div. Time Scale: 2 ms / div. BPL Average Voltage = 14.40 V. BPH Average Voltage = 14.72 V.

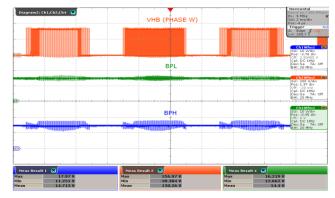


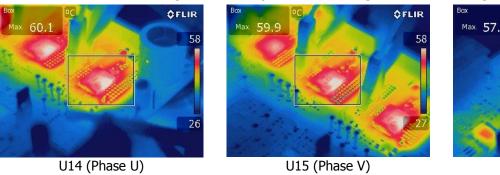
Figure 34 – INL and /INH Signal at 300 W Load. CH2: V_{HB_PHASEW} , 200 V / div. CH4: V_{BPL} , 10 V / div. CH1: V_{BPH} , 10 V / div. Time Scale: 2 ms / div. BPL Average Voltage = 14.40 V. BPH Average Voltage = 14.71 V.



7.3 **Thermal Performance**

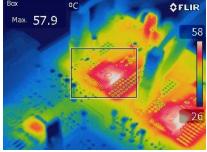
The thermal scans below depict on-board device thermal performance after 30 minutes of operation with 300 W inverter output power running at a constant speed of 5000 RPM, 12 kHz PWM switching frequency, and at room ambient temperature.

7.3.1 100 W Loading Condition (300 mA Average Motor Winding RMS Current)



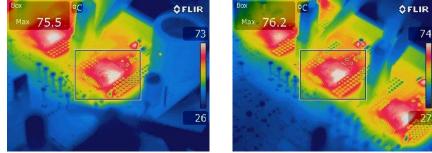
 $T_{case(U1)} = 60.1 \ ^{\circ}C$

T_{case(U2)} = 59.9 °C



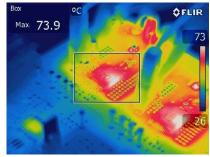
U16 (Phase W) $T_{case(U3)} = 57.9 \ ^{\circ}C$

7.3.2 200 W Loading Condition (635 mA Average Motor Winding RMS Current)



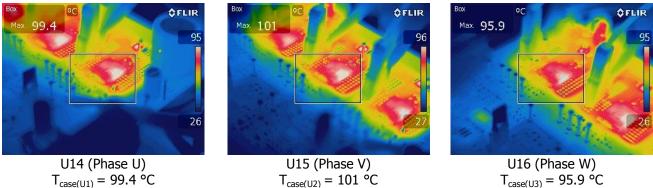
U14 (Phase U) $T_{case(U1)} = 75.5 \ ^{\circ}C$

U15 (Phase V) $T_{case(U2)} = 76.2 \ ^{\circ}C$



U16 (Phase W) $T_{case(U3)} = 73.9 \text{ °C}$

300 W Loading Condition (920 mA Average Motor Winding RMS Current) 7.3.3



 $T_{case(U3)} = 95.9 \ ^{\circ}C$

Figure 35 – BridgeSwitch Device Case Temperatures at 100 W, 200 W, and 300 W Output Power.



7.4 No-Load Input Power Consumption

The graph below shows the BridgeSwitch 3-phase inverter no-load input power taken at different input voltage. Voltage was measured directly at the positive input of C24 (bulk capacitance) bypassing F1 and RT1. The aux circuit, current sense amplifier, and microcontroller no-load input power were not included. This can be achieved by deactivating the aux circuit for accurate measurement of the BridgeSwitch no-load input power. In order to deactivate the aux circuit component U5, D6, and L2 were depopulated.

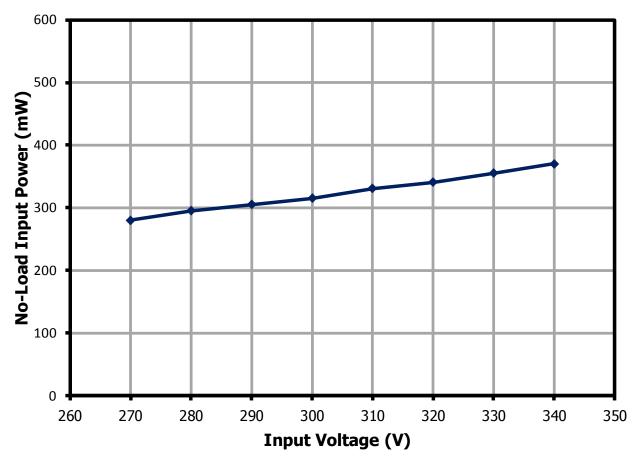


Figure 36 – No-Load Input Power.



7.5 Efficiency

The graph and table below shows the BridgeSwitch inverter efficiency at 340 VDC input, 12 kHz PWM switching frequency, and a constant motor speed of 5000 RPM. The aux circuit, current sense amplifier, microcontroller, input fuse F1, and thermistor RT1 power consumption are not included for efficiency data accuracy. This is accomplished by measuring the input voltage directly at the positive input of C24 (bulk capacitance) bypassing F1 and RT1. Aux circuit was also bypassed by depopulating component U5, D6, and L2. External 5 VDC supply was provided between pins +5V and GND for microcontroller and current sense amplifier.

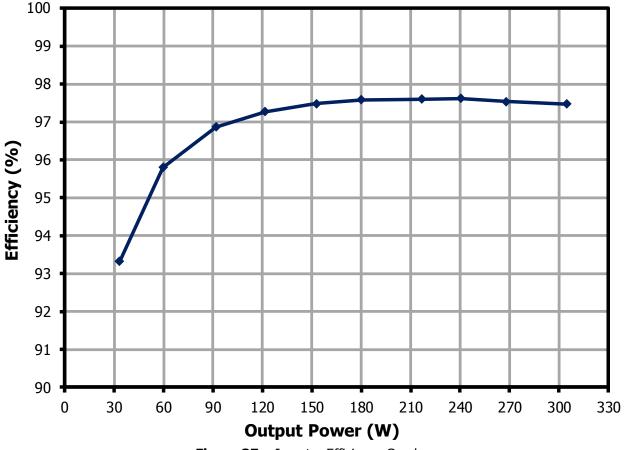


Figure 37 – Inverter Efficiency Graph.





DC Input Voltage (V _{IN})	Input DC Current (mA)	PF	Input Power (W)	I _{RMS} U (mA)	I _{RMS} V (mA)	I _{RMS} W (mA)	Inverter Output Power (W)	Inverter Efficiency (%)
339	99.11	0.97	32.57	96	100	102	30.43	93.5
341	190.19	0.99	63.93	190	194	196	61.63	96.4
341	278.50	0.99	93.95	281	285	286	91.38	97.3
341	375.86	0.99	127.08	381	384	386	124.13	97.7
341	465.67	0.99	157.65	481	484	486	154.16	97.8
341	551.04	0.99	186.76	557	559	562	182.84	97.9
341	629.39	1.00	213.44	635	638	641	208.99	97.9
341	740.92	1.00	251.42	746	748	750	246.06	97.9
341	816.72	1.00	277.18	825	827	829	271.13	97.8
341	920.48	1.00	312.49	923	927	925	305.35	97.7

Table 2 – Efficiency Table.



7.6 Device and System Level Protection / Monitoring

7.6.1 Overcurrent Protection (OCP)

The waveforms below show the current limit triggering of the BridgeSwitch device. For this test current set resistors R_{XL} and R_{XH} were adjusted to 115 k Ω and 5 5 k Ω value resulting to a current limit of approximately 1.1 A and 2.4 A respectively.

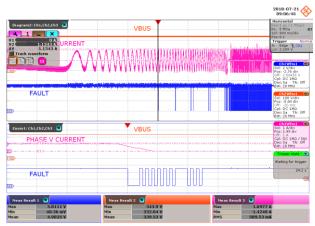


Figure 38 – OCP at R_{XL}/R_{XH} =115k Ω , I_{LIM} =1.1 A. CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 500 ms / div. Time Scale (Zoomed Area): 100 µs / div. FAULT Flag Reading = 0000010.

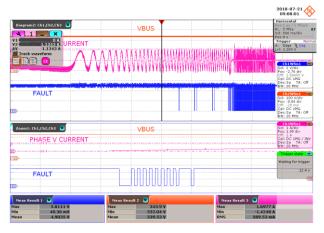
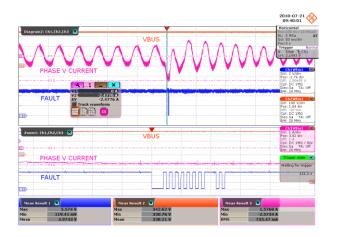


Figure 39 – OCP Fault Clear at R_{XL}/R_{XH} =115k Ω .

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 500 ms / div. Time Scale (Zoomed Area): 100 μ s / div. FAULT Clear = 0000000.



 $\label{eq:Figure 40-OCP at R_{XL}/R_{XH}=55k\Omega, \ I_{LIM}=2.4A. \\ CH2: \ V_{BUS}, \ 100 \ V \ / \ div. \\ CH2: \ I_{PHASE}, \ 1 \ A \ / \ div. \\ CH1: \ V_{FAULT}, \ 2 \ V \ / \ div. \\ Time \ Scale: \ 50 \ ms \ / \ div. \\ Time \ Scale \ (Zoomed \ Area): \ 100 \ \mu s \ / \ div. \\ FAULT \ Flag \ Reading \ = \ 0000010. \\ \end{array}$

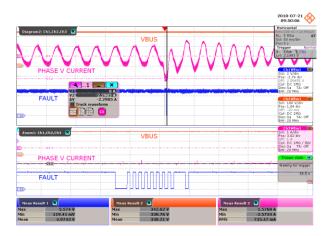


Figure 41 – OCP Fault Clear at R_{XL}/R_{XH} =55k Ω .

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASEr} 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zoomed Area): 100 µs / div. FAULT Flag Reading = 0000000.



7.6.2 Thermal Warning and Shutdown

The waveforms below depict the low-side FREDFET over-temperature warning and shutdown function. A localized external heat source was applied to the device to force temperature rise.





Figure 42 – Thermal Warning at 100 W. CH2: I_{PHASE} , 500 mA / div. CH1: V_{FAULT} , 4 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 ns / div. FAULT Flag/Reading = 0000100.

MM

Figure 44 – Thermal Shutdown at 100 W.

CH1: V_{FAULT}, 4 V / div.

Time Scale: 2 s / div.

CH3: V_{FAULT}, 500 mA / div.

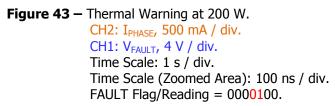
Time Scale (Zoomed Area): 150 μ s / div.

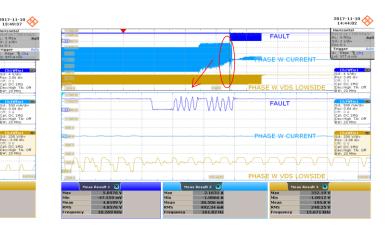
FAULT Flag/Reading = 0001000.

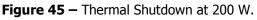
CH4: V_{FAULT}, 200 V / div.

FAUL

FAULT





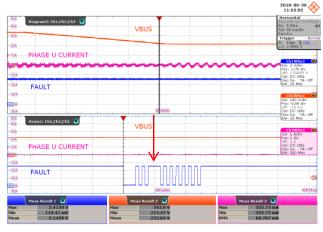


CH1: V_{FAULT} , 4 V / div. CH3: V_{FAULT} , 500 mA / div. CH4: V_{FAULT} , 200 V / div. Time Scale: 2 s / div. Time Scale (Zoomed Area): 150 μ s / div. FAULT Flag/Reading = 0001000.



7.6.3 Undervoltage (UV)

The test results below demonstrate the integrated bus UV monitoring function and status reporting through the communication bus (FAULT pin). Device U2 senses the bus voltage through resistors R5, R8, and R13.



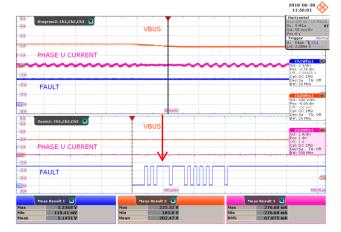


Figure 46 – UVP, 3000 RPM, No-Load, 340 V to 220 V. CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zoomed Area): 100 µs / div. UV Level = 100%.

FAULT Flag Reading = 0100000.

Figure 47 – UVP, 3000 RPM, No-Load, 220 V to 190 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zoomed Area): 100 µs / div. UV Level = 85%. FAULT Flag Reading = 0110000.

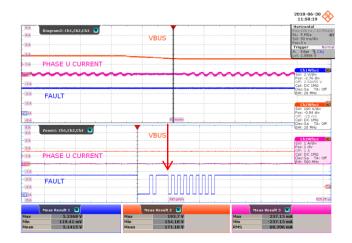


Figure 48 – UVP, 3000 RPM, No-Load, 190 V to 160 V. CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zoomed Area): 100 µs / div. UV Level = 70%. FAULT Flag Reading = 1000000.

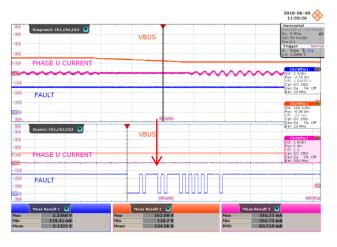


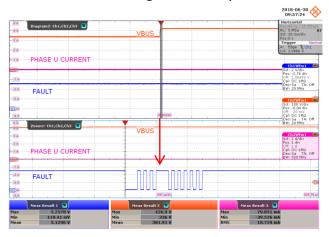
Figure 49 – UVP, 3000 RPM, No-Load, 160 V to 120 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zoomed Area): 100 µs / div. UV Level = 55%. FAULT Flag Reading = 1010000.



7.6.4 *Overvoltage (OV)*

The waveforms below illustrate the bus OV monitoring feature. The bus sensing resistance is set at 7 M Ω (total value of R5, R8, and R13) giving an over voltage (OV) level threshold to 422 VDC. The BridgeSwitch device stops switching and reports the OV fault condition as soon as the bus voltage exceeds the OV threshold. Switching resumes after the bus voltage level drops below the OV detection threshold.



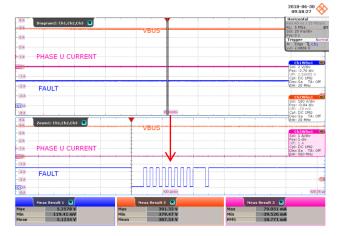


Figure 50 – OVP, 0 RPM, 340 V to 425 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 µs / div. Measured OVP Level = 426.90 V. FAULT Flag/Reading = 0010000. Figure 51 – OVP, 0 RPM, 425 V to 340 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 μ s / div. OV Fault Clear. FAULT Flag/Reading = 0000000.



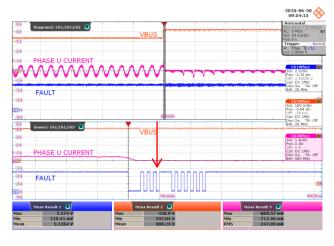


Figure 52 – OVP, 5000 RPM, 100 W, 340 V to 425 V. CH2: V_{BUS}, 100 V / div. CH2: I_{PHASE}, 1 A / div. CH1: V_{FAULT}, 2 V / div.

Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 μ s / div. Measured OVP Level = 426.90 V. FAULT Flag/Reading = 0010000.

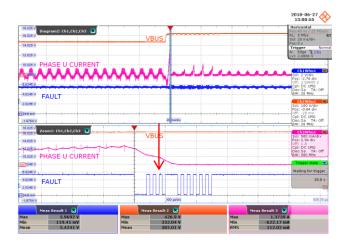


Figure 54 – OVP, 5000 RPM, 200 W, 340 V to 425 V. CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 µs / div. Measured OVP Level = 426.90 V. FAULT Flag/Reading = 0010000.

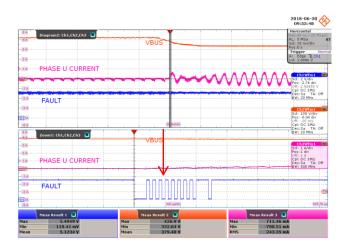


Figure 53 - OVP, 5000 RPM, 100 W, 425 V to 340 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 µs / div. OV Fault Clear. FAULT Flag/Reading = 0000000.



Figure 55 – OVP, 5000 RPM, 200 W, 425 V to 340 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 µs / div. OV Fault Clear. FAULT Flag/Reading = 0000000.



7.6.5 System Thermal Fault

The waveforms below show the system thermal warning flag of the BridgeSwitch device through an external thermistor RT2. The device checks the resistance connected to the SM pin every 1 second for a period of 10 ms. The system temperature fault was simulated by applying a localized external heat to sense thermistor RT2 with the motor running at different loading condition.



Figure 56 – System Thermal Fault, 0 RPM, No-Load. CH2: V_{BUS}, 100 V / div. CH2: I_{PHASE}, 1 A / div. CH1: V_{FAULT}, 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 μ s / div. FAULT Flag/Reading = 1100000.

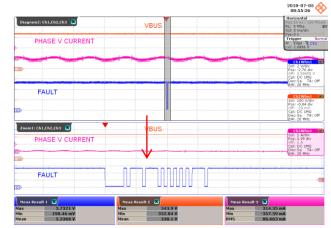


Figure 57 – System Thermal Fault, 5000 RPM ,Light Load.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 µs / div. FAULT Flag/Reading = 1100000.



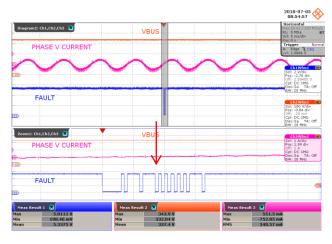


Figure 58 – System Thermal Fault, 5000 RPM, 100 W. CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div.

CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 μ s / div. FAULT Flag/Reading = 1100000.

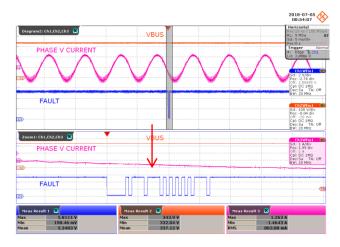


Figure 60 – System Thermal Fault, 5000 RPM, 300 W. CH2: V_{BUS} , 100 V / div. CH2: I_{PHASEr} 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 µs / div. FAULT Flag/Reading = 1100000.

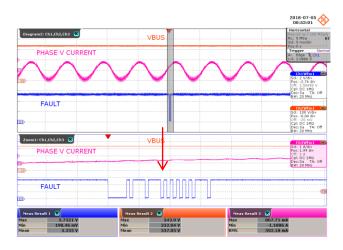


Figure 59 – System Thermal Fault, 5000 RPM, 200 W.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 µs / div. FAULT Flag/Reading = 1100000.

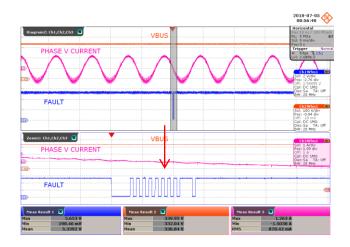


Figure 61 – System Fault Clear, 5000 RPM, 300 W.

CH2: V_{BUS}, 100 V / div. CH2: I_{PHASE}, 1 A / div. CH1: V_{FAULT}, 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 μ s / div. FAULT Flag/Reading = 0000000.



7.7 Fault Monitoring Through UART

F = FAULT FW = FAULT WARNING FS = FAULT SHUTDOWN FN = FAULT NONE

F: 1, 4 1 = BrSw Device ID 4 = FAULT

FAULT CLEAR	0
OVER VOLTAGE	4
UV 100%	2
UV 85%	6
UV 70%	1
UV 55%	5
SYSTEM THERMAL FAULT	3
LS DRIVER FAULT	7
DEVICE THERMAL WARNING	10
DEVICE THERMAL SHUTDOWN	8
HS DRIVER FAULT	18
LS OVER CURRENT	20
HS OVER CURRENT	40



7.7.1 Overcurrent Protection (OCP)

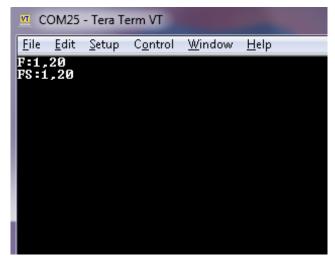


Figure 62 – LS OCP, $R_{XL}/R_{XH} = 115 \text{ k}\Omega$, $I_{LIM} = 1.1 \text{ A}$. Tera Term Reading: F: 1, 20 = BrSw Device 1, LS OCP Fault. FS: 1, 20 = Shutdown.

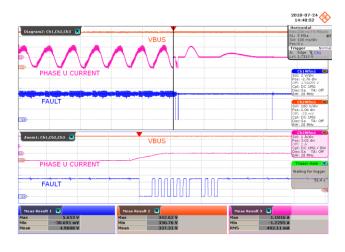


Figure 63 – LS OCP , R_{XL}/R_{XH} = 115 k Ω , I_{LIM} = 1.1 A. CH2: V_{BUS}, 100 V / div.

CH2: V_{BOS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed Area): 100 µs / div. FAULT Flag Reading = 0000010.

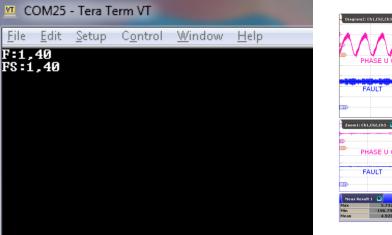


Figure 64 – HS OCP, $R_{XL}/R_{XH} = 115 \text{ k}\Omega$, $I_{LIM} = 1.1 \text{ A}$. Tera Term Reading: F: 1, 40 = BrSw Device 1, LS OCP Fault. FS: 1, 40 = Shutdown.

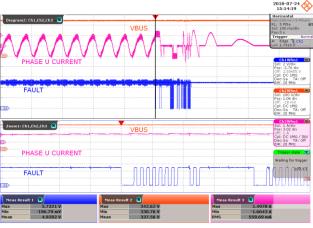


Figure 65 – HS OCP, $R_{XL}/R_{XH} = 115 \text{ k}\Omega$, $I_{LIM} = 1.1 \text{ A}$. CH2: V_{BUS} , 100 V / div.

CH2: V_{BOS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed Area): 100 µs / div. FAULT Flag Reading = 0000001.



7.7.2 Undervoltage (UV)

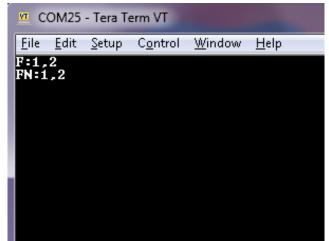


Figure 66 – UVP, 3000 RPM, No-Load, 340 V to 220 V. Tera Term Reading: F: 1, 4 = BrSw Device 1, Undervoltage (100%) Fault. FN: 1, 4 = No Action.

<u>v</u> C	OM25	- Tera Te	erm VT			
	<u>E</u> dit	<u>S</u> etup	C <u>o</u> ntrol	<u>W</u> indow	<u>H</u> elp	
F:1, FW:1	6					

Figure 68 – UVP, 3000 RPM, No-Load, 220 V to 190 V. Tera Term Reading: F: 1, 6 = BrSw Device 1, Undervoltage (85%) Fault. FW: 1, 6 = Warning.

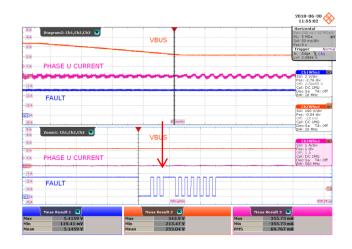


Figure 67 – UVP, 3000 RPM, No-Load, 340 V to 220 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zoomed Area): 100 Ω s / div. UV Level = 100%. FAULT Flag Reading = 0100000.

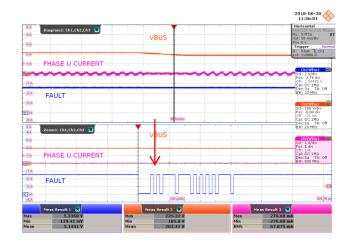


Figure 69 – UVP, 3000 RPM, No-Load, 220 V to 190 V. CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zoomed Area): 100 µs / div.

Time Scale (Zoomed Area): 100 μ s / div. UV Level = 85%. FAULT Flag Reading = 0110000.



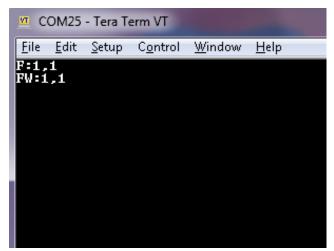


Figure 70 – UVP, 3000 RPM, No-Load, 190 V to 160 V. Tera Term Reading: F: 1, 1 = BrSw Device 1, Undervoltage (70%) Fault. FW: 1, 1 = Warning

<u>File Edit Setup Control Window Help</u>

COM25 - Tera Term VT

F:1,5 FW:1,5

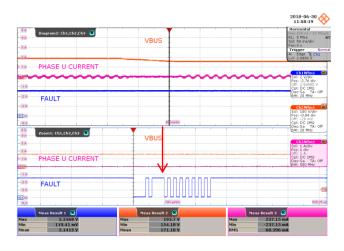


Figure 71 – UVP, 3000 RPM, No-Load, 190 V to 160 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zoomed Area): 100 µs / div. UV Level = 70%. FAULT Flag Reading = 1000000.

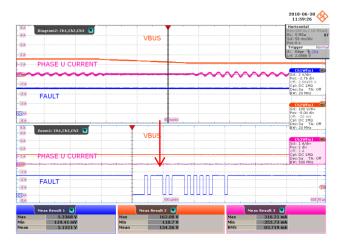


Figure 72 – UVP, 3000 RPM, No-Load, 160 V to 120 V. Tera Term Reading: F: 1, 5 = BrSw Device 1, Undervoltage (55%) Fault. FW: 1, 5 = Warning

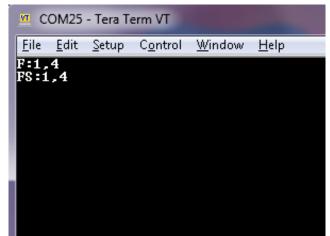
Figure 73 – UVP, 3000 RPM, No-Load, 160 V to 120 V. CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 50 ms / div. Time Scale (Zeemed Area): 100 us / div.

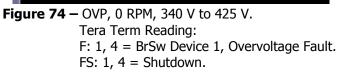
Time Scale (Zoomed Area): 100 μ s / div. UV Level = 55%. FAULT Flag Reading = 1010000.





7.7.3 Overvoltage (OV)





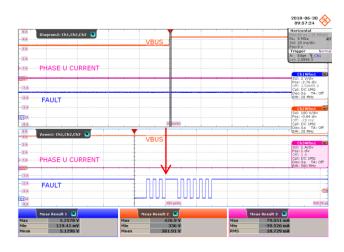


Figure 75 – OVP, 0 RPM, 340 V to 425 V.

CH2: V_{BUS} , 100 V / div. CH2: I_{PHASE} , 1 A / div. CH1: V_{FAULT} , 2 V / div. Time Scale: 1 s / div. Time Scale (Zoomed Area): 100 µs / div. Measured OVP Level = 426.90 V. BrSw FAULT Flag/Reading = 0011100.



7.8 Abnormal Testing

This paragraph provides results during abnormal operation tests for appliances with motors as described in IEC 60335-1 (Safety of household and similar electrical appliances). The tests include:

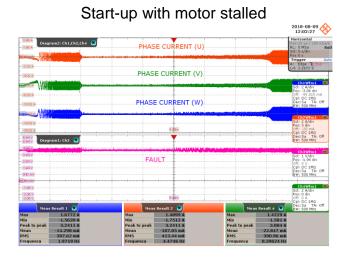
- Operation under stalled motor conditions
- Operation with one motor winding disconnected
- Running overload test

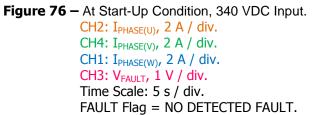
The test results demonstrate the integrated protection features of the BridgeSwitch under such abnormal operations.

7.8.1 Operation Under Stalled (Motor) Conditions

The figures below demonstrate the motor phase currents and fault flag during start-up with motor at stalled condition. For start-up motor stalled condition, the motor break was set at maximum load condition to prevent the motor from rotating. The tests was done at different input voltages starting from 340 VDC down to 200 VDC to demonstrate fault condition occurrence.

For the running motor stalled condition, the inverter is initially running at 340 VDC, 300 W output load, and a motor speed of 5000 RPM. The load was then ramped up drastically to simulate sudden break or sudden stoppage of motor rotation.





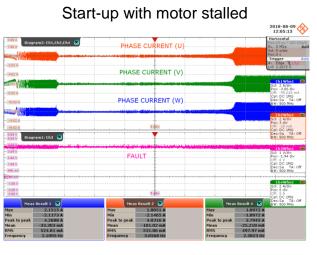
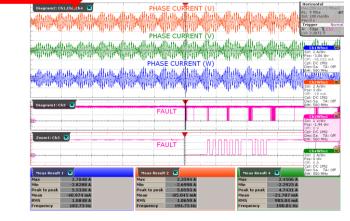


Figure 77 – At Start-Up Condition, 300 VDC Input.

 $\begin{array}{l} \mbox{CH2: I}_{PHASE(U)}, \mbox{ 2 A / div.} \\ \mbox{CH4: I}_{PHASE(V)}, \mbox{ 2 A / div.} \\ \mbox{CH1: I}_{PHASE(W)}, \mbox{ 2 A / div.} \\ \mbox{CH3: V}_{FAULT}, \mbox{ 1 V / div.} \\ \mbox{Time Scale: 5 s / div.} \\ \mbox{FAULT Flag = NO DETECTED FAULT.} \end{array}$



Start-up with motor stalled Diagram2: Ch1,Ch2,Ch4 PHASE CURRENT (U) PHASE CURRENT (V) PHASE CURRENT (W) am 1: Ch 3 💌 FAULT



Zoomed Version



Time Scale: 5 s / div.

Figure 79 – At Start-up Condition, 250 VDC Input, Zoomed Version. CH2: $I_{PHASE(U)}$, 2 A / div. CH4: I_{PHASE(V)}, 2 A / div. CH1: I_{PHASE(W)}, 2 A / div. CH3: V_{FAULT} , 1 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed FAULT): 100 µs / div. 1^{st} FAULT Flag = 0000010.

Zoomed Version

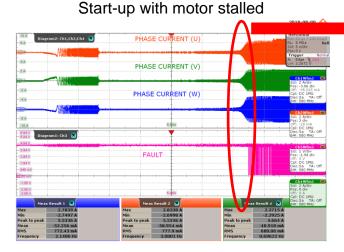


Figure 80 – At Start-up Condition, 200 VDC Input. CH2: $I_{PHASE(U)}$, 2 A / div.

CH4: I_{PHASE(V)}, 2 A / div. CH1: I_{PHASE(W)}, 2 A / div. CH3: V_{FAULT}, 1 V / div. Time Scale: 5 s / div.

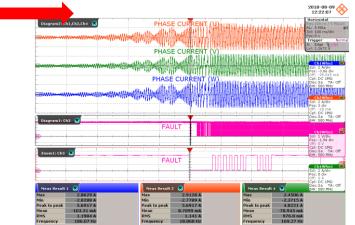


Figure 81 – At Start-up Condition, 200 VDC Input, Zoomed Version. CH2: I_{PHASE(U)}, 2 A / div.

CH4: I_{PHASE(V)}, 2 A / div. CH1: I_{PHASE(W)}, 2 A / div. CH3: V_{FAULT}, 1 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed FAULT): 100 µs / div. 1^{st} FAULT Flag = 0000010, LS FET Over-Current.



Running condition then motor stalled

		2	118-08-10 🔬
Diagram2: Ch1,Ch2,Ch4 🔀	PHASE CURRENT (U)	Rat Rat Sci Pos	s:10 µs / 100 kSa SMSa R :Ss/div 110 s igger Norr
	PHASE CURRENT (V)	Al evi	Edge 2 Ch3 2.2672 V
	PHASE CURRENT (W)		Ch1Wfm1 cl: 2 A/div os: -3.06 div ff: -95.015 mA pl: DC 1MQ ec:Sa TA: Off W: 500 MHz
Diagram 1: Ch3			Ch2Wfm1 C cl: 2 A/div sc: 3 div ff: -20 mA pl: DC 1MQ ec:Sa TA: Off W: S00 MHz
	FAULT	B	Ch3Wfm1 cl: 1 V/div os: -1.94 div ff: 0 V pl: DC 1MQ ec:Sa TA: Off W: 500 MHz
			Ch4Wfm1 C cl: 2 A/div os: 0 div ff: 0 A pl: DC 1MQ ec:SA TA: Off
Meas Result 1 X fax 2.7048 A A iin -3,145 A A eak to peak 5.8499 A A tean 10.307 mA A VMS 1.089 A F requency 167.22 Hz A	Mess Result 2 X Max 2,7547 A Min -2,8579 A Peak to peak 5,6126 A Mean -132.3 mA RMS 1,0075 A Frequency 167,722 Hz	Meas 2.4500 Å Min -2.8458 Å Peak to peak 5.2964 Å Mean -80.153 mÅ RMS 910.24 mÅ Frequency 167.96 Hz	W: 500 MHz

Figure 82 – At Running Condition, 340 VDC Input, 300 W Loading Condition. CH2: I_{PHASE(U)}, 2 A / div.

CH2: $I_{PHASE(U)}$, 2 A / div. CH4: $I_{PHASE(V)}$, 2 A / div. CH1: $I_{PHASE(W)}$, 2 A / div. CH3: V_{FAULT} , 1 V / div. Time Scale: 5 s / div.

Zoomed Version

Figure 83 – At Running Condition, 340 VDC Input, 300 W Loading Condition, Zoomed Version.

CH2: $I_{PHASE(U)}$, 2 A / div. CH4: $I_{PHASE(V)}$, 2 A / div. CH1: $I_{PHASE(W)}$, 2 A / div. CH3: V_{FAULT} , 1 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed FAULT): 100 µs / div. 1st FAULT Flag = 0000010, LS FET Over-Current



7.8.2 *Operation with One Motor Phase/Winding Disconnected*

The figures below depict the motor phase currents and fault flag during operation with one motor winding disconnected. One phase is disconnected during running condition at 100 W, 200 W, and 300 W load (at 340 VDC input, and a motor speed of 5000 RPM). Reconnection of phase was also tested per loading condition to determine the robustness of the BridgeSwitch inverter. No damage was incurred in the motor as well as in the BridgeSwitch inverter during and after the test.

One Phase Disconnected at 100 W The second state of the second s

Figure 84 – At Running Condition, 340 VDC Input. CH2: $I_{PHASE(U)}$, 2 A / div. CH4: $I_{PHASE(V)}$, 2 A / div. CH1: $I_{PHASE(W)}$, 2 A / div. CH3: V_{FAULT} , 1 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed FAULT): 100 µs / div. FAULT Flag = NONE. One Phase Reconnected at 100 W

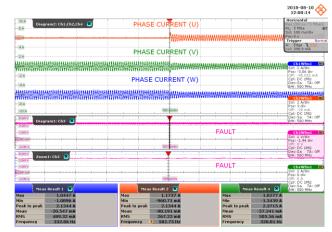
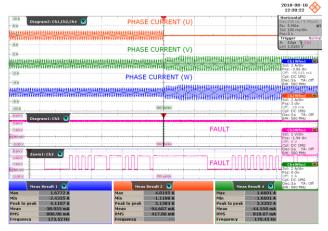


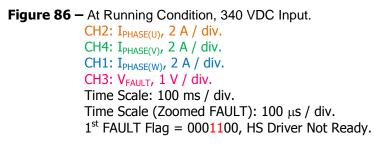
Figure 85 – At Running Condition, 340 VDC Input.

CH2: $I_{PHASE(U)}$, 2 A / div. CH4: $I_{PHASE(V)}$, 2 A / div. CH1: $I_{PHASE(W)}$, 2 A / div. CH3: V_{FAULT} , 1 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed FAULT): 100 µs / div. FAULT Flag = NONE.



One Phase Disconnected at 200 W





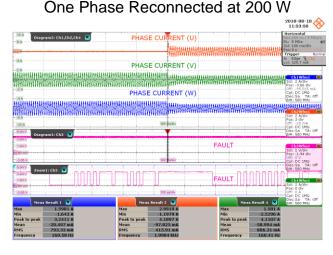
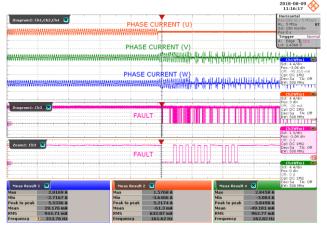


Figure 87 – At Running Condition, 340 VDC Input.

CH2: $I_{PHASE(U)}$, 2 A / div. CH4: $I_{PHASE(V)}$, 2 A / div. CH1: $I_{PHASE(W)}$, 2 A / div. CH3: V_{FAULT} , 1 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed FAULT): 100 µs / div. 1st FAULT Flag = 0001100, HS Driver Not Ready.



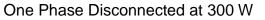


Figure 88 – At unning Condition, 340 VDC Input. CH2: I_{PHASE(U)}, 2 A / div. CH4: I_{PHASE(V)}, 2 A / div.

CH1: I_{PHASE(W)}, 2 A / div.

CH3: V_{FAULT}, 2 V / div. Time Scale: 100 ms / div.

Time Scale (Zoomed FAULT): 100 μ s / div.

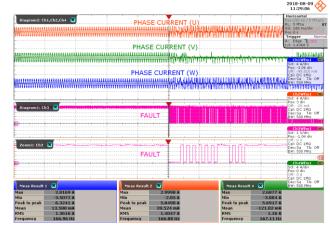
1st FAULT Flag = 0000010, LS FET Over-Current.

Note: During 300 W loss of phase condition the motor stops rotating or at stalled condition even when the phase is reconnected.



7.8.3 Running Overload Test

The figures below depict the motor phase currents and status update flag during a running overload fault condition. During this test, the motor load is increased such that the current through the motor windings increases by 10% and until steady conditions are established. The load is then increased again and the test repeats until the BridgeSwitch protection engages or the motor stalls. During the overload condition, the motor is non-operational with no device or motor damage.



Overload Test >300 W

Figure 89 – At Running Condition, 340 VDC Input. CH2: $I_{PHASE(U)}$, 2 A / div. CH4: $I_{PHASE(V)}$, 2 A / div. CH1: $I_{PHASE(W)}$, 2 A / div. CH3: V_{FAULT} , 2 V / div. Time Scale: 100 ms / div. Time Scale (Zoomed FAULT): 100 µs / div. 1st FAULT Flag = 0000010, LS FET Over-Current

Note: During overload condition the motor stops rotating or at stalled condition.



8 Appendix

8.1 Board Quick Reference / Guide

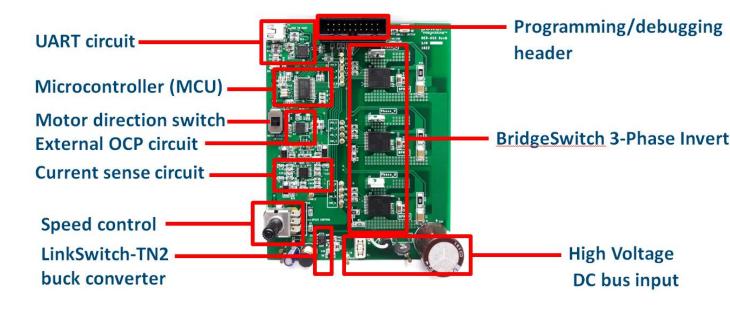


Figure 90 – DER-653 Board Quick Reference / Guide.



8.2 **Recommended Start-up Sequence**

BridgeSwitch devices have internal self-supply supporting commutation PWM frequencies up to 20 kHz. To ensure sufficient supply voltage levels across the BPL pin capacitor and the BPH pin capacitor at inverter start-up, the system micro-controller (MCU) should follow the recommended power-up sequence as depicted below.

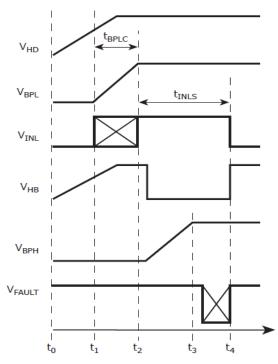


Figure 91 – Recommended Power-up Sequence with Self-Supplied Operation.

The table below lists activities occurring during the recommended power-up sequence.

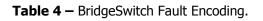
Time Point	Activity
t _o	High-voltage DC bus is applied
t1	 Internal current source starts charging BPL pin capacitor once HD pin voltage reaches V_{HD(START)} System MCU may start setting low-side power-FREDFET control signal INL to high
t2	 BPL pin voltage reaches V_{BPL} (typ. 14.5 V) Device determines external device settings Internal Gate drive logic turns on low-side power FREDFET after device setup completes and once INL becomes high or if it is high already Internal current source charges BPH pin capacitor
t ₃	 BPH pin voltage reaches V_{BPH} with respect to HB pin (typically 14.5 V) Device starts communicating successful power-up through fault pin Note: The device does not send a status update if the internal power-up sequence did not complete successfully
t4	 BridgeSwitch is ready for state operation (indicated by communicated status update at time point t₃) System MCU turns off low-side FREDFET

Table 3 – Power-up Sequence with Self-Supplied Operation.



Status	Parameter	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
High-voltage bus OV	I _{ov}	0	0	1	х	х	x	х
High-voltage bus UV 100%	I _{UV100}	0	1	0	x	x	x	X
High-voltage bus UV 85%	I _{uves}	0	1	1	x	х	x	x
High-voltage bus UV 70%	I _{UV70}	1	0	0	х	x	x	X
High-voltage bus UV 55%	I _{UV55}	1	0	1	x	x	x	х
System thermal fault	V _{TH(TM)}	1	1	0	x	х	x	х
LS Driver not ready ¹	n/a	1	1	1	х	x	x	х
LS FET thermal warning	T _{WA}	х	x	х	0	1	x	х
LS FET thermal shutdown	T _{SD}	x	x	х	1	0	x	X
HS Driver not ready ²	I _{COM}	х	x	х	1	1	x	X
LS FET over-current	V _{X(TH)}	x	x	х	Х	x	1	x
HS FET over-current	V _{X(TH)}	х	x	х	х	х	x	1
Device Ready (no faults)	n/a	0	0	0	0	0	0	0

8.3 Status Word Encoding



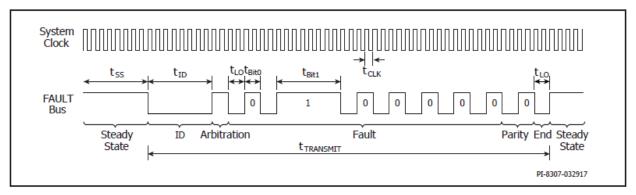


Figure 92 – Fault Status Communication Bit Stream.



8.4 **Programming the TMPM375 Microcontroller (MCU)**

Below are the step-by-step procedures in programming the microcontroller:

- 8.4.1 Installing IAR Embedded Workbench for ARM
 - a. Go to https://www.iar.com/
 - b. Download the IAR Embedded Workbench for ARM through the following link:

https://www.iar.com/iar-embedded-workbench/#!?currentTab=free-trials

- c. After downloading, install the software and follow the instructions.
- d. When you start IAR Embedded Workbench for the first time, the License Wizard will open. Choose Register with IAR Systems to get an evaluation license (the internet access is needed).

License Wizard	X
Welcome	
This wizard will help you to activate your IAR Embedd ARM license.	led Workbench for
C If you have a license number, enter it here:	
Use a network license Register with IAR Systems to get an evaluation	license
Don't run the Wizard for this product at starture	EIAR SYSTEMS
< Back	Next > Cancel

- e. Click **Register**, choose a time or code size limited evaluation license, and then register to get your license number, which will be delivered to you via e-mail within a few minutes.
- f. Activate the license in the License Wizard window.
- g. You may register both the time or code size limited evaluation licenses, active and switch in between from the **License Manager**.
- h. For the latest updates on software and documentation, please visit <u>www.iar.com/kit updates</u>.



8.4.2 Debugger / Programmer

- a. In order to program the microcontroller, a debugger is needed.
- b. The debugger is available for purchase in the following link:

https://store.iar.com/product/I-jet





8.4.3 Setting up the DER-653 Board for Programming

a. Connect your computer and the programmer using the USB-micro cable. Do not connect the programmer to the evaluation board yet.



b. The "USB" LED on the front side of the programmer will lit with green once Windows completes searching for a USB driver.



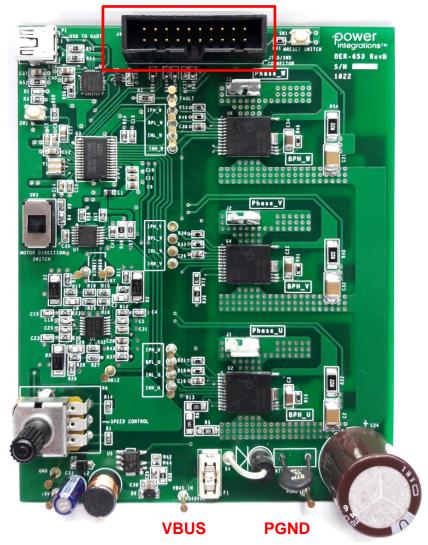
- c. Connect the programmer to the JTAG connector J4.
- d. Supply the board with 20 VDC on VBUS and PGND pin.



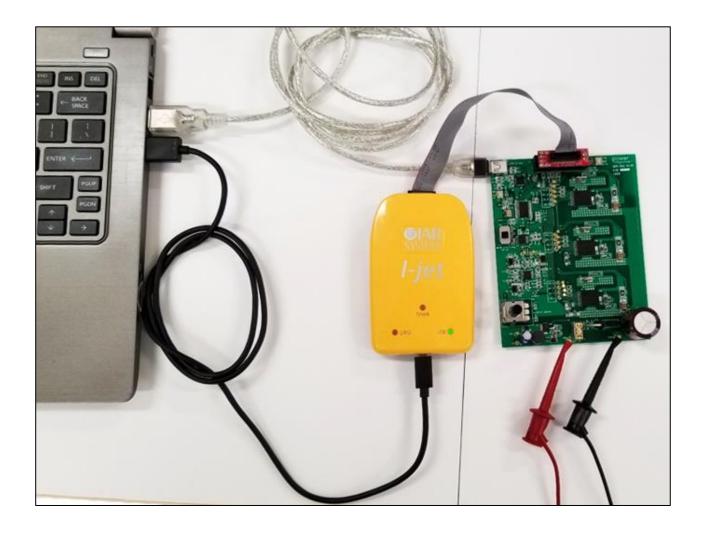




JTAG CONNECTOR



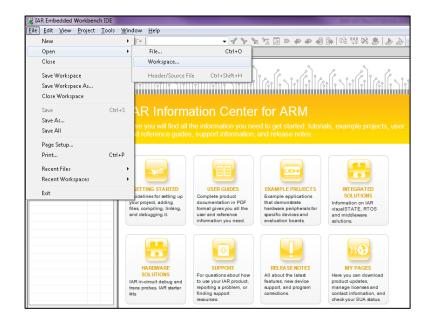






8.4.4 *Programming and Running the BLDC Motor Code*

- a. Download the program. (This step is required only if you need to reprogram the Toshiba MCU. By default, the DER-653 comes preprogrammed with the BLDC motor code and is ready to use.)
- b. Save the workspace file in a desired folder.
- c. Start/run the IAR Embedded Workbench.
- d. Click File -> Open -> Workspace

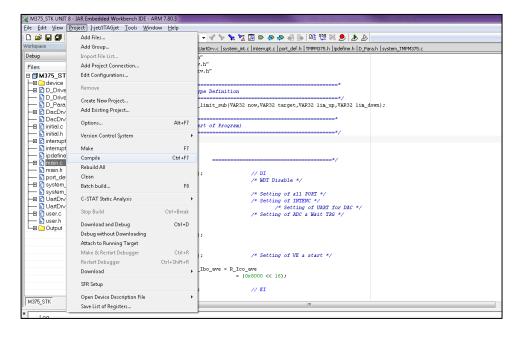


e. Locate the workspace file (downloaded code) – see example below:

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f. After opening the workspace file, go to Project -> Compile:



g. Go to Project -> Make:

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D_Para	Create New Project	limit_sub(VAR32 now,VAR32 target,VAR32 lim_up,VAR32 lim_down);
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initial.h	Version Control System	*/
interrupt	Make F7	
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UantDrv	Stop Build Ctrl+Break	/* Setting of URAT for DRC */ /* Setting of ADC & Wait TRG */
user.h	Download and Debug Ctrl+D	
-B Cuput	Debug without Downloading	
	Attach to Running Target	
	Make & Restart Debugger Ctrl+F	; /* Setting of VE & start */
	Restart Debugger Ctrl+Shift+F	
	Download	<pre>Libo_ave = R_Ico_ave = (0x8000 << 16);</pre>
	SFR Setup	// EI
WOTE OTK	Open Device Description File	•
M375_STK	Save List of Registers	m
× Mossagos		



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		/* Setting of all PORT */
UartDr.	,	/* Setting of INTERC */ /* Setting of UART for DAC */
🕂 🕀 💽 user.c	Stop Build Ctrl+Break	/* Setting of ADC & Wait TRG */
user.h	Download and Debug Ctrl+D	
	Debug without Downloading	
	Attach to Running Target	
	Make & Restart Debugger Ctrl+R); /* Setting of VE & start */
	Restart Debugger Ctrl+Shift+R	, , , , , , , , , , , , , , , , , , ,
	Download +	<pre>Ibo_ave = R_Ico_ave</pre>
	SFR Setup	// EI
ļ	Open Device Description File	// ***
M375_STK	Save List of Registers	m
×		

h. To program the microcontroller go to Project -> Download and Debug:

i. Click the **Start** button to start the application.



j. Turn OFF the VBUS DC supply (0V).

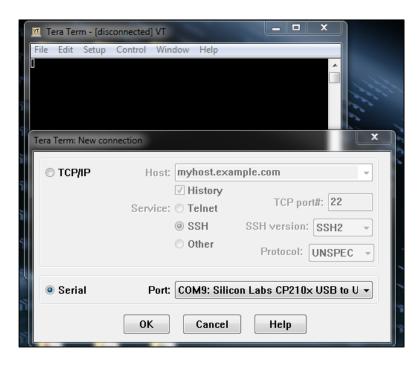


8.5

1. Download the TERA TERM software. <u>https://osdn.net/projects/ttssh2/releases/</u> **NOTE:** Be careful there may be many unwanted links showing download, start now, or others so be sure to select and click 4.92 file)

About Tera Term	23
Tera Term Version 4.92 (SVN# 6484) OK	
Includes: Oniguruma 5.9.6 Tera Term Pro version 2.3 + IPv6 0.81 Mar 10, 1998 T. Teranishi Copyright (C) 1994-1998 T. Teranishi (C) 2004-2016 TeraTerm Project All Rights Reserved.	
Built using Microsoft Visual C++ 8.0 build 50727 Build time: Aug 31 2016 21:17:50 Author: <u>https://ttssh2.osdn.jp/</u> Forum: <u>http://logmett.com/support-forums</u>	

- 2. Configure the connection settings (When connecting Tera Term interface please make sure VCC power is ON (VCC = 5 V) and USB is connected to PC
- 3. Prompt menu for New Connection will appear
- 4. Select Serial pull down menu to Silicon Labs from , click "OK"

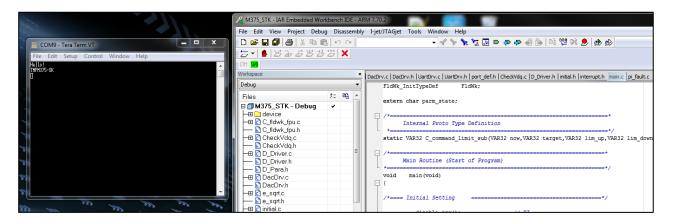




- 5. Select; Set-Up menu
 - -Choose Port
 - Select Baud Rate: 57600 (TMPM365)
 - Press "OK"

💆 COM9 - Tera Term VT		×
File Edit Setup Control	l Window Help	
0		
Tera Term: Serial port set	tup	×
Port:	сомя -	ОК
Baud rate:	57600 -	
Data:	8 bit 🔫	Cancel
Parity:	none 🔻	
Stop:	1 bit 🗸	Help
	T DR •	
Flow control:	none 🔻	
-		
Transmit dela	у	
0 mse	c/char 0	msec/line

- 6. Open IAR Embedded Work bench, select and run program
- 7. When successful connection is established, you will see: "Hello! TMPM365-SK" in Tera Term screen.





8. Sample readings:

🗵 C	ом9 -	Tera Te	rm VT			- 0	x
File	Edit	Setup	Control	Window	Help		
Hello! THPH37 F:1,1d F:1,1d F:1,19 F:1,19 F:1,1e F:1,1e F:1,1a F:1,1a	5-SK						
							~



Fault	Fault ID	Action/Decision
HV bus 0ver Voltage	001xxxx	Shutdown
HV 100%	010xxxx	Warning
HV bus 85%	011xxxx	Warning
HV bus 70%	100xxxx	Warning
HV bus 55%	101xxxx	Warning
System Thermal	110xxxx	Shutdown
LS Driver Not Ready	111xxxx	Shutdown
LS FET Thermal Warning	xxx010x	Warning
LS FET Thermal Shutdown	xxx10xx	Shutdown
LS FET Over Current	xxxxx1x	Shutdown
HS Driver Not Ready	xxx11xx	Shutdown
HS FET Over Current	xxxxx1	Shutdown
Device Ready	0000000	None

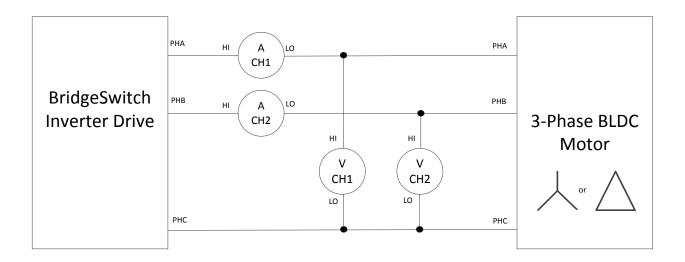
8.6 **Microcontroller Action/Decision To BridgeSwitch Fault Conditions**



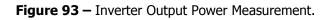


8.7 **Inverter Output Power Measurement**

The 3-phase inverter output power (P_{OUT}) measurement uses the "two wattmeter" method as illustrated below.



$$P_{OUT} = P_{CH1} + P_{CH2}$$





8.8 Current Capability vs. Ambient Temperature

Figure 94 depicts the continuous RMS current capability of the DER-653 example design under different operation conditions: Either 6 kHz or 12 kHz PWM frequency and the three BRD1165C devices operating self-supplied or with external supply at their respective BPL- and BPH-pins. Each curve details the available continuous RMS current at different board ambient temperatures with a package temperature of 100 °C (average of all three devices).

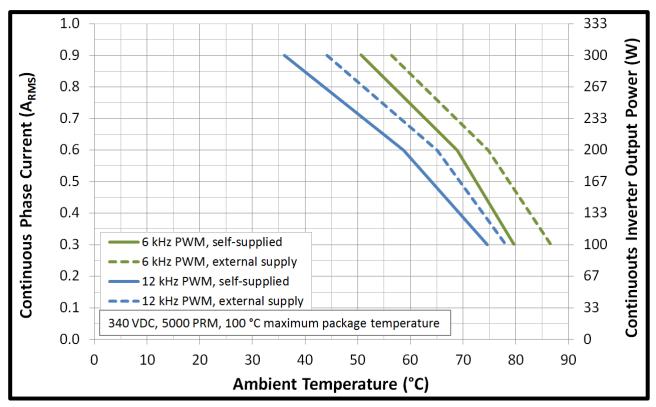


Figure 94 - Current Capability vs. Ambient Temperature (Max. 100 °C Package Temperature).



8.9 FOC Motor Tuning Considerations for Toshiba TMP375FSDMG Microcontroller (VEMCU)

FOC represents one of the most advanced motor control methods in controlling Brushless Sensorless motors to achieve optimal efficiency, noise, torque ripple, and dynamic responses at an affordable cost, which are usually not possible by other means.

Unlike operation with sensor-based motors, users need to have knowledge of the sensorless motor's parameters such as motor resistance and inductance. More importantly, users must also know about the close-loop control parameters defined as Proportional and Integral Gains (PI loop control gains) at a given range of operating conditions. As a result, this reference design will work specifically with motor 57BL115S30-3150TF9 as the motor parameters are programmed into the TMPM375FDSMG VEMCU.

If users plan to use the DER-653 board for different motors, the motors need to be tuned (i.e. motor parameters and PI control gains needed). Toshiba has the Parameter Tuning System (PTS) tool that can assist users to extract the information but it requires the PTS tuning to be done at user's facilities. Since technical support is needed, users should contact their local Toshiba office for further information. Alternatively, users can send inquiries to Toshiba_Vector_Engine_MCU_Inquiry and the inquiries will be directed to the right contacts for assistance.



8.10 Test Bench Set-up

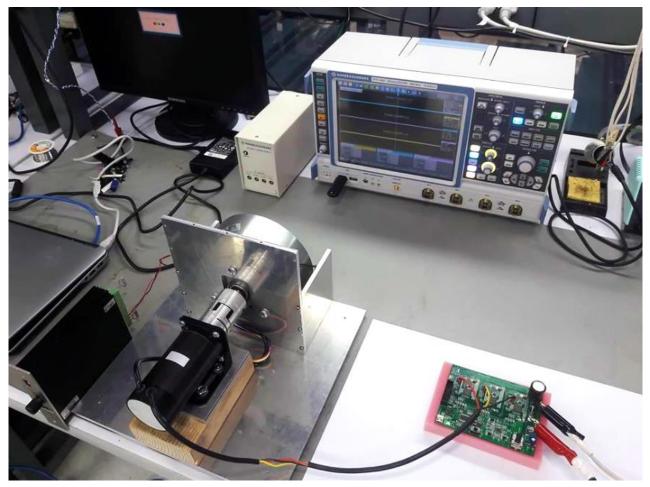


Figure 95 – Actual Bench Set-up.

EQUIPMENT USED:

- 1. Motor 300 W, 5000 RPM, Model: 57BL110S30-3150TF0
- 2. **Motor break load** 24 VDC, 300 W motor brake load, Model: HB-503B by China-Tension
- 3. **Break load control** 24 VDC, 500 mA break load control, Model: ICS-500 by China-Tension
- 4. Coupler 8 mm X 17 mm motor coupler
- 5. **High voltage DC source** Agilent 6812B, used for supplying 340 VDC to the 3-phase inverter
- 6. **Low voltage DC souce** Technique QT3005D-3 power supply, used supplying 24 VDC for break load control.



9 Revision History

Date	Author	Rev.	Description & Changes	Approval
13-Nov-18	JMQC	1.0	Initial Release.	Apps & Mktg
01-Feb-19	КМ	1.1	Updated Section 8.4.4	
05-Aug-19	KM	1.2	Added Section 8.6, 8.8 and 8.9.	



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