



Design Example Report

Title	<5 mW (Including 1 mW Pre-Load) No-Load Input Power, 8 W Standby Power Supply Using LinkZero™-LP LNK576DG
Specification	85 VAC – 265 VAC Input; 5 V, 1.6 A Output
Application	Standby Power Supply For LCD TVs and Appliances
Author	Applications Engineering Department
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Revision	1.3

Summary and Features

- Ultra low no-load consumption, <5 mW at 230 VAC with 1 mW pre-load
- EcoSmart™ – 70% average efficiency, exceeds standards requirement of 67%, and thus meets all existing and proposed harmonized energy efficiency standards including: CECP (China), CEC, EPA, AGO, European Commission

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <<http://www.powerint.com/ip.htm>>.

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Important Note:

Although this board was designed to satisfy safety isolation requirements, it has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the power supply.



1 Introduction

This report describes a universal input, 5 V, 1.6 A flyback power supply using a LinkZero-LP family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer along with test data and oscilloscopes of important electrical waveforms.

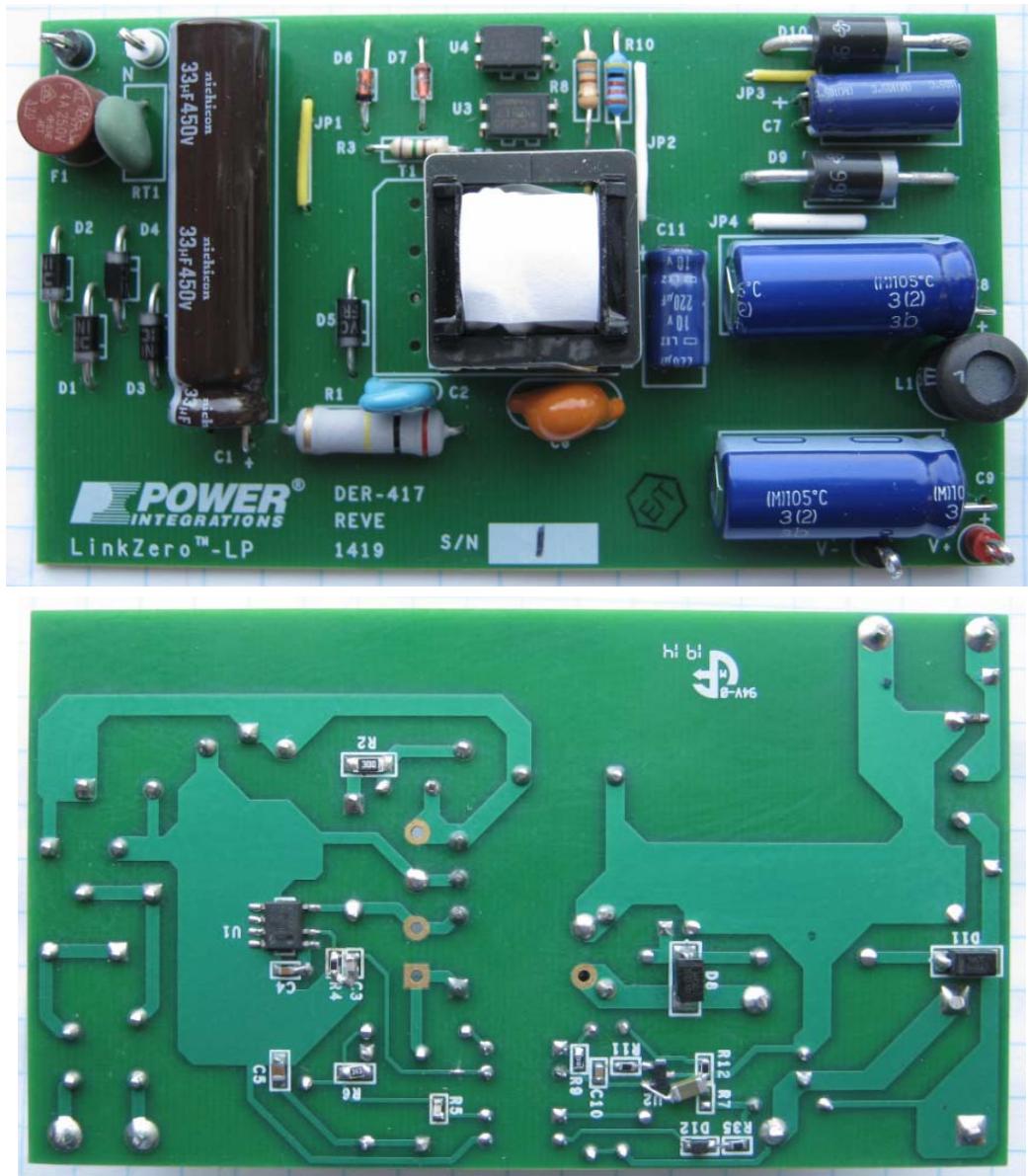


Figure 1 – Populated Circuit Board Photographs.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Input Power (1 mW Output Load)				<5	mW	230 VAC (2)
Output						
Output Voltage	V_{OUT}		5		V	See V-I Curves, Figure 11, for limits
Output Ripple Voltage (pk-pk)	V_{RIPPLE}			50	mV	20 MHz bandwidth (1)
Output Current	I_{OUT}		1.6		A	
Total Output Power						
Continuous Output Power	P_{OUT}			8	W	
Ambient Temperature	T_{AMB}	-5		65	°C	Free convection, sea level

Notes:

- 1) 5 ms / div. LeCroy 606Zi
- 2) Yokogawa WT210 (30 min warm up time 30 min integration time).



3 Circuit Diagram

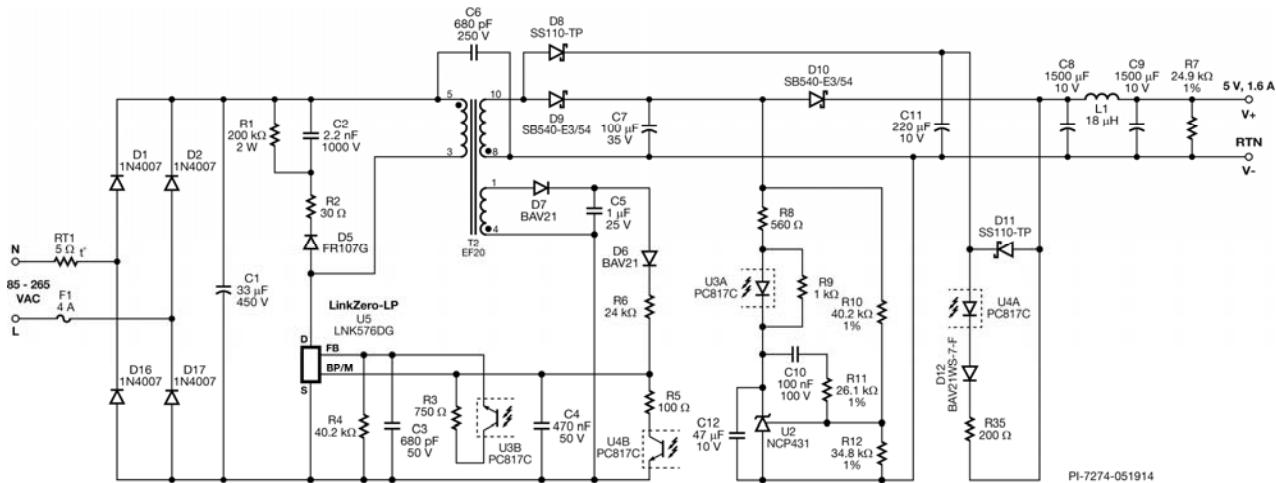


Figure 2 – Schematic.



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4 Circuit Description

4.1 Input Rectification

Diodes D1-D2, D16-D17 rectifies the AC input which is then filtered by capacitor C35. In some applications, additional reduction in no-load or light load input power can be achieved by disconnecting capacitor C1 using a relay. When the capacitor is disconnected from the circuit, reduction in input power is achieved due to elimination of capacitor leakage current which contributes to the loss. If this reduction of loss is not required capacitor C1 can be kept in the circuit at all times.

4.2 LinkZero-LP Primary:

The LinkZero-LP device (U5) integrates an oscillator, an ON/OFF controller, start-up and protection circuitry and a power MOSFET all on one monolithic IC.

One side of the power transformer primary is connected to the positive leg of C1 and the other side is connected to the DRAIN (D) pin of U5. At the start of a switching cycle, the controller turns the MOSFET ON, and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold, the controller turns the MOSFET OFF. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor.

4.3 Primary Clamp

The clamp network formed by C2, R1, R2, and D5 limits the drain voltage (preventing spikes at MOSFET turn off) and dissipates transformer leakage inductance energy.

4.4 Output Rectification

Output rectification is provided by diode D9 and capacitor C7 as well as D10 and the output pi filter network composed of C8, L1 and C9.

4.5 Ultra-low No-load Input Power

The LinkZero-LP device has a built in “power-down” (PD) mode wherein when 416 consecutive switching cycles have been skipped, the chip goes into the PD mode and inhibits switching and in addition, dramatically reduces its internal power consumption. The PD mode occurs when the output load has reduced to about 0.3% of full load. During PD mode the internal circuitry of the device completely shuts down and thus the capacitor connected to BYPASS (BP) pin C4 is discharged from 5.8 V. The controller wakes up to check output load conditions at a frequency determined by the user through the choice of the BP pin capacitor value. Once the BP pin voltage reaches 3 V, U5 powers up again and resumes switching. If the load increases such that fewer than 416 cycles were skipped, the IC resumes normal operation.



When U5 is in PD mode, the time taken for the BP pin voltage to discharge to VBPPDRESET (~3 V) determines the duration of the PD off-time. The duration of the PD off-time also determines the ripple on the output voltage. The total energy stored in C5 and C4 determine the PD off-time (and also the output ripple in PD mode).

4.6 Feedback

The output voltage is sensed through resistor divider R10 and R12 and fed back to U5 through the NCP431 at U2 and optocoupler U3. Switching cycles are skipped if the FB pin disable threshold voltage (1.7 V) is exceeded. When the sensed voltage at the FB pin falls below the disable threshold, switching cycles are re-enabled. By adjusting the ratio of enabled to disable switching cycles, output regulation is maintained.

At increased loads, beyond the output power limiting point, the FB pin voltage begins to reduce as the power supply output voltage falls. As the FB pin voltage falls, the switching frequency reduces to provide some output current limiting. When the FB pin voltage drops below the auto-restart threshold (typically 0.9 V on the FB pin), the power supply enters the auto-restart mode. In this mode, the power supply will turn off for 1.2 s and then turn back on for 170 ms. The auto-restart function reduces the average output current during an output short-circuit condition.

4.7 Output Switch-Capacitor for Light Load Performance Improvement

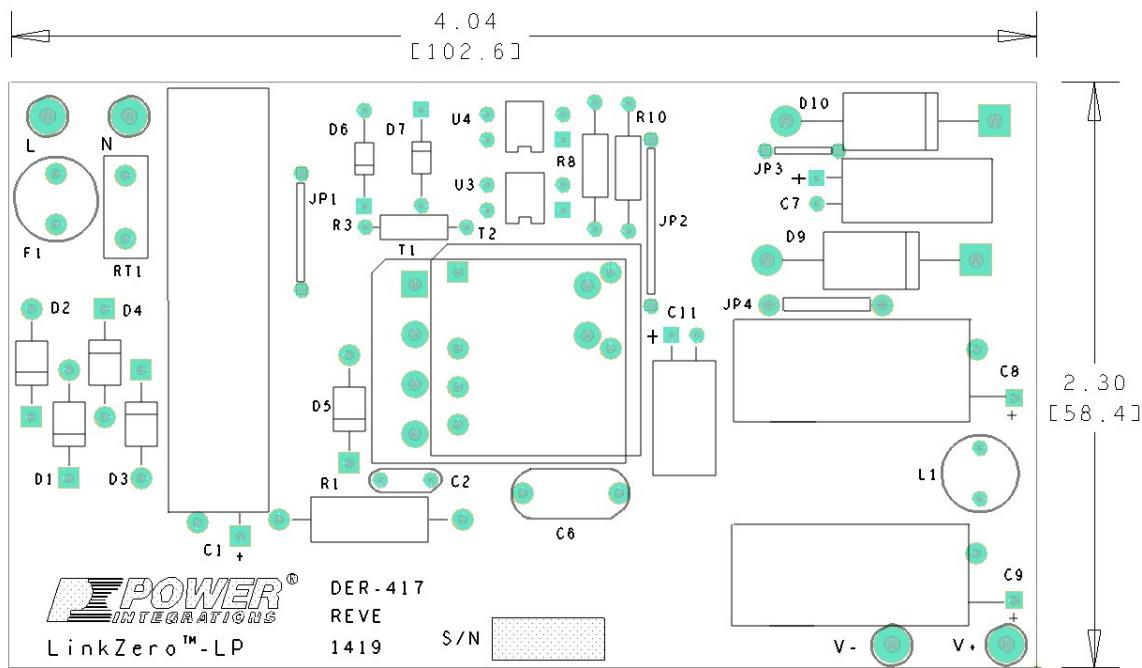
This design uses a special arrangement of components consisting of D10, and the pi filter composed of C8, L1 and C9 on the secondary side to achieve very low no load input power. Diode D9 and capacitor C7 is the main output rectifier filter. Output voltage of the power supply is sensed across C7. Capacitor C7 has a low capacitance. The additional rectifier diode D10 isolates the pi filter from the main rectification of D9 and C7. The π filter provides for a low ripple output voltage. During normal operation, loss in diode D10 can result in loss of efficiency and also drop in output voltage due to diode losses.

This design also uses special circuit formed by components D6, C11, D11, U4, D12 and R35 to wake up the IC to normal load when the power supply is in PD mode.

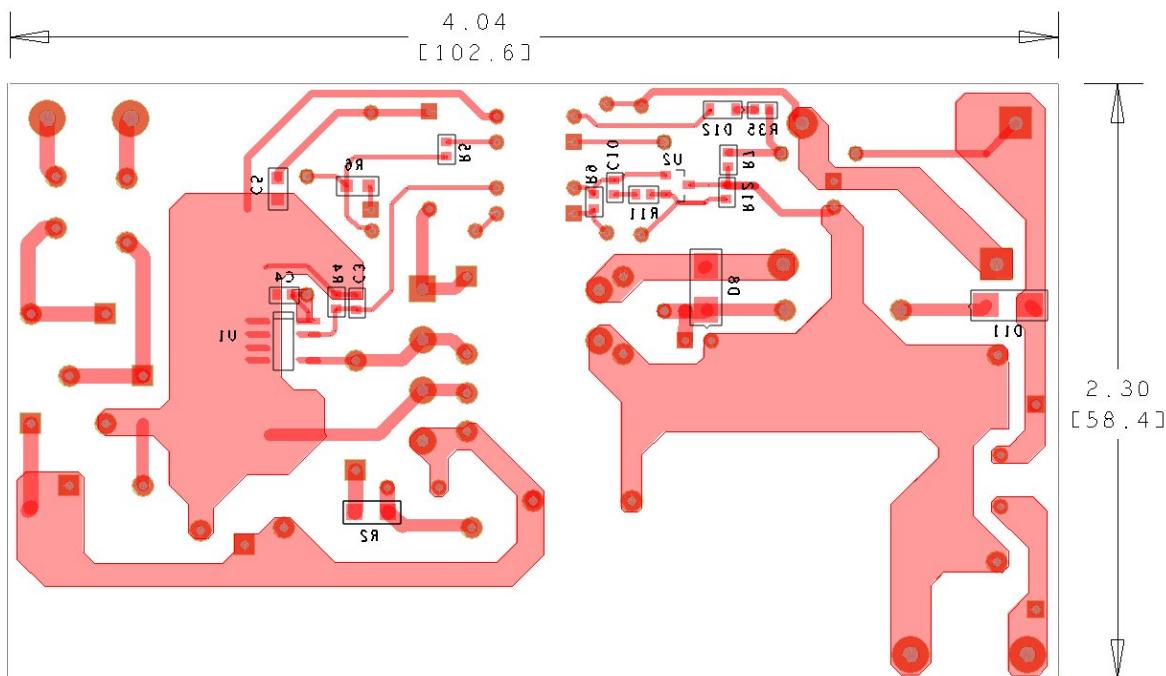
During PD mode C11 is charged through D6 and D11, the potential difference across U4A, D12, and R35 is negligible, however, as soon as load is connected to the power supply, the voltage at the output drops and the potential difference across U4A, D12 and R35 becomes large enough to pull current through the optocoupler which pulls the BP pin of U5 low to wake it up from PD mode and avoid a large undershoot in the output voltage.



5 PCB Layout



Top View.



Bottom View

Figure 3 – Printed Circuit Board Layout (Dimensions in Inches).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	33 μ F, 450 V, Electrolytic ,(10 x 42)	UPZ2W330MND9	Nichicon
2	1	C2	2.2 nF, 1 kV, Ceramic, SL, 0.2" L.S.	DEBB33A222KA2B	Murata
3	1	C3	680 pF 100 V, Ceramic, NPO, 0603	CGA3E2C0G2A681J	TDK
4	1	C4	470 nF, 50 V, Ceramic, X7R, 0603	UMK107B7474KA-TR	Taiyo Yuden
5	1	C5	1 μ F, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
6	1	C6	680 pF, Ceramic, Y1	440LT68-R	Vishay
7	1	C7	100 μ F, 35 V, Electrolytic, Low ESR, 180 m Ω , (6.3 x 15)	ELXZ350ELL101MF15D	Nippon Chemi-Con
8	2	C8 C9	1500 μ F, 10 V, Electrolytic, Low ESR, 45 m Ω , (10 x 25)	ELXZ100ELL152MJ25S	Nippon Chemi-Con
9	1	C10	100 nF 100 V, Ceramic, X7R, 0603	GRM188R72A104KA35D	Murata
10	1	C11	220 μ F, 10 V, Electrolytic, Low ESR, 250 m Ω , (6.3 x 11.5)	ELXZ100ELL221MFB5D	Nippon Chemi-Con
11	1	C12	47 μ F, 10 V, Ceramic, X5R, 1206	C1206C476M8PACTU	Kemet
12	4	D1 D2 D3 D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
13	1	D5	1000 V, 1 A, Fast Recovery Diode, GP DO-41	FR107G-B	Rectron
14	2	D6 D7	250 V, 250 mA, Fast Switching, DO-35	BAV21	Vishay
15	2	D8 D11	100 V, 1 A, Schottky, DO-214AC (SMA)	SS110-TP	Micro commercial
16	2	D9 D10	40 V, 5 A, Schottky, DO-201AD	SB540-E3/54	Vishay
17	1	D12	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
18	1	F1	4 A, 250 V, Fast, TR5	37014000410	Wickman
19	1	JP1	Wire Jumper, Insulated, #24 AWG, 0.5 in	C2003A-12-02	Gen Cable
20	1	JP2	Wire Jumper, Non-insulated, #22 AWG, 0.8 in	298	Alpha
21	1	JP3	Wire Jumper, Insulated, #24 AWG, 0.4 in	C2003A-12-02	Gen Cable
22	1	JP4	Wire Jumper, Insulated, TFE, #18 AWG, 0.5 in	C2052A-12-02	Alpha
23	2	L V-	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
24	1	L1	18 μ H, 1.6 A, 9 x 12 mm H	AIUR-03-180K	Abracor Corp
25	1	N	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
26	1	R1	200 k Ω , 5%, 2 W, Metal Oxide	RSF200JB-200K	Yageo
27	1	R2	30 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ300V	Panasonic
28	1	R3	750 Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-750R	Yageo
29	1	R4	40.2 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4022V	Panasonic
30	1	R5	100 Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
31	1	R6	24 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ243V	Panasonic
32	1	R8	560 Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-560R	Yageo
33	1	R9	1 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1001V	Panasonic
34	1	R10	40.2 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-40K2	Yageo
35	1	R11	26.1 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2612V	Panasonic
36	1	R12	34.8 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3482V	Panasonic
37	1	R13	24.9 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
38	1	R35	200 Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2000V	Panasonic
39	1	RT1	TKS Thermistor, 5 Ω , 3 A	SCK08053MSY	Thinking Elect.
41	1	T2	Bobbin, EF20, Horizontal, 10 pins		
42	1	U1	LinkZero-LP, SO-8-DN	LNK576DG	Power Integrations
43	1	U2	2.4 V Shunt Regulator IC, 1%, 0 to 70C, SOT-23-3	NCP431ACSNT1G	ON Semi
44	2	U3 U4	Optocoupler, 35 V, CTR 200-300%, 4-DIP	PC817C	Sharp
45	1	V+	Test Point, RED,THRU-HOLE MOUNT	5010	Keystone

Note – All parts are RoHS compliant



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7 Transformer Specification

7.1 Electrical Diagram

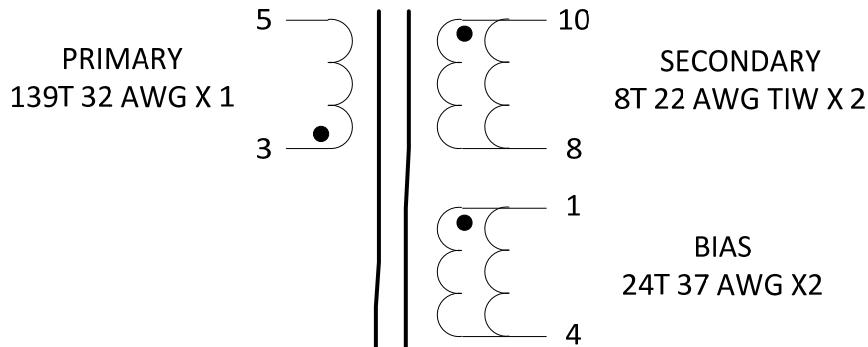


Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 Hz 1 second, from pins 1, 3, 4, 5 to pins 8, 10	3000 VAC
Nominal Primary Inductance	Measured at 1 V pk-pk, typical switching frequency, between pin 3 to pin 5, with all other windings open.	2617 μ H
Tolerance	Tolerance of primary inductance.	$\pm 5\%$
Maximum Primary Leakage	Measured between pin 3 to pin 5, with all other windings shorted.	78 μ H

7.3 Materials

Item	Description
[1]	Core: EF20, PC40EF20-Z ,gapped for ALG of 112 nH/T ²
[2]	Bobbin EF20, Horizontal, 10 pins (5/5), PI # 25-00834-00
[3]	Barrier Tape: Polyester film [1 mil (25 μ m) base thickness], 10.00 mm wide.
[4]	Varnish.
[5]	Magnet Wire: #32 AWG and #37 AWG, Solderable Double Coated.
[6]	Triple Insulated Wire: #22 AWG.

7.4 Transformer Build Diagram

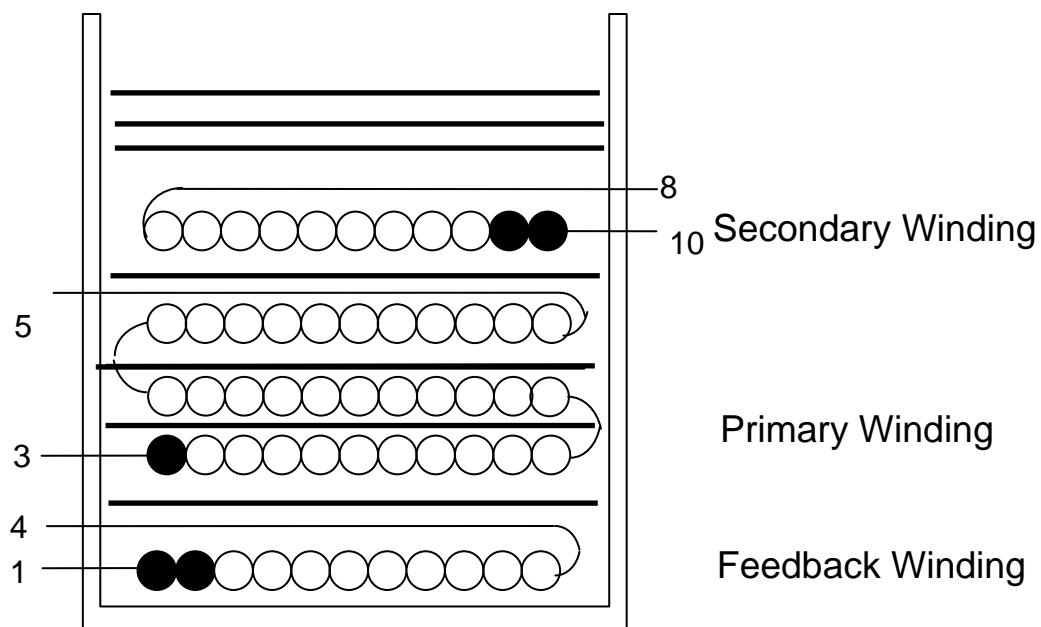


Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

Bias Winding	Start on pin(s) 1 and wind 26 turns (x 2 filar) of item [5]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 4. Add 1 layer of tape, item [3], for insulation.
Primary Winding	Start on pin(s) 3 and wind 145 turns (x 1 filar) of item [5] in 3 layer(s) from left to right. At the end of 1st layer, continue to wind the next layer from right to left. At the end of 2nd layer, continue to wind the next layer from left to right. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 5. Add 1 layer of tape, item [3], for insulation.
Secondary Winding	Start on pin(s) 10 and wind 8 turns (x 2 filar) of item [6]. Spread the winding evenly across entire bobbin. Wind in same rotational direction as primary winding. Finish this winding on pin(s) 8. Add 2 layers of tape, item [3], for insulation.
Core Assembly	Assemble and secure core halves. Item [1].
Varnish	Dip varnish uniformly in item [4]. Do not vacuum impregnate.



8 Transformer Design Spreadsheet

<i>ACDC_LinkZero-LP_041114; Rev.1.2; Copyright Power Integrations 2014</i>	<i>INPUT</i>	<i>INFO</i>	<i>OUTPUT</i>	<i>UNIT</i>	<i>ACDC_LinkZero-LP_041114_Rev1-2.xls; LinkZero-LP Flyback Transformer Design Spreadsheet</i>
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.5			Volts	Output Voltage (main) measured at the end of output cable (For CV/CC designs enter typical CV tolerance limit)
IO	1.56			Amps	Power Supply Output Current (For CV/CC designs enter typical CC tolerance limit)
PO		Warning	8.58	Watts	!!! For UNIVERSAL INPUT : REDUCE PO<8W (use larger LinkZero-LP, or reduce input voltage range)
Feedback Type	OPTO		Opto		Choose 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback from the 'Feedback Type' drop down box at the top of this spreadsheet
Clampless design	NO		External Clamp		Choose 'YES' from the 'Clampless Design' drop down box at the top of this spreadsheet for a clampless design. Choose 'NO' to add an external clamp circuit. Clampless design lowers the total cost of the power supply
n	0.68		0.68		Efficiency Estimate at output terminals. For CV only designs enter 0.7 if no better data available
Z			0.5		Loss Allocation Factor (Secondary side losses / Total losses)
tC	2.9			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	33		33.00	uFarads	Input Capacitance
Input Rectification Type	F		F		Choose H for Half Wave Rectifier and F for Full Wave Rectification from the 'Rectification' drop down box at the top of this spreadsheet
ENTER LinkZero-LP VARIABLES					
LinkZero-LP	LNK576		LNK576		LinkZero-LP device.
Chosen Device		LNK576			
ILIMITMIN			0.325	Amps	Minimum Current Limit
ILIMITMAX			0.375	Amps	Maximum Current Limit
fSmin			93000	Hertz	Minimum Device switching Frequency. May be lower than 93 kHz for high line (230 V only) designs
I^2fMIN			10562	A^2Hz	I^2f Minimum value (product of current limit squared and frequency is trimmed for tighter tolerance)
I^2fTYP			12250	A^2Hz	I^2f typical value (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	104		104	Volts	Reflected Output Voltage
VDS			10	Volts	LinkZero-LP on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP		Info	0.59		!!! Info. INCREASE KP > 0.9 (Increase VOR, Larger input capacitor)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EF20		EF20		User-Selected transformer core
Core		EF20		P/N:	PC40EF20-Z
Bobbin		EF20_BOBBIN		P/N:	EF20_BOBBIN
AE			0.335	cm^2	Core Effective Cross Sectional Area
LE			4.49	cm	Core Effective Path Length
AL			1570	nH/T^2	Ungapped Core Effective Inductance
BW			12.2	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary)



					Creepage Distance)
L	3		3		Number of primary layers
NS	8		8		Number of Secondary Turns
NB			23		Number of Bias winding turns. Calculation is made assuming that Bias winding is first winding on bobbin to achieve lowest cost
VB			17.25	Volts	Bias Winding Voltage
R1			N/A	k-ohms	Upper Resistor in the resistor divider component between bias winding and FB pin of LinkZero-LP. Calculated to be a standard 1% value
R2			N/A	k-ohms	Lower Resistor in the resistor divider component between bias winding and FB pin of LinkZero-LP. Calculated to be a standard 1% value
RPB			68.00	k-ohms	Optional BP pin resistor (connected between BP pin and bias winding) to improve efficiency. Calculated to be a standard 5% value
CBIAS			220.00	nF	Bias Winding capacitor
CFB			680.00	pF	FB pin resistor (To improve noise sensitivity)
CBP			220.00	nF	BP pin capacitor. Value of CBP influences Power Down period. See datasheet for details
Recommended Bias Diode			1N4003		Place this diode on the return leg of the bias winding for optimal EMI.
DC INPUT VOLTAGE PARAMETERS					
VMIN			95	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.59		Maximum Duty Cycle
IAVG			0.15	Amps	Average Primary Current
IP			0.33	Amps	Minimum Peak Primary Current
IR			0.19	Amps	Primary Ripple Current
IRMS			0.19	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2617	uHenries	Typical Primary Inductance. +/- 7%
LP_TOLERANCE	7		7	%	Primary inductance tolerance
NP			139		Primary Winding Number of Turns
ALG			136	nH/T^2	Gapped Core Effective Inductance
BM		Info	2110	Gauss	!!! Info. Flux densities above ~ 2000 Gauss may produce audible noise. Verify with dip varnished sample transformers. Increase NS to greater than or equal to 9 turns or increase VOR
BAC			424	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1675		Relative Permeability of Ungapped Core
LG			0.31	mm	Gap Length (Lg > 0.08 mm)
BWE			36.6	mm	Effective Bobbin Width
OD			0.26	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.21	mm	Bare conductor diameter
AWG			32	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			64	Cmils	Bare conductor effective area in circular mils
CMA			340	Cmils/Amp	Primary Winding Current Capacity (150 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			5.63	Amps	Peak Secondary Current
ISRMS			2.95	Amps	Secondary RMS Current
IRIPPLE			2.50	Amps	Output Capacitor RMS Ripple Current



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CMS			589	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			22	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.65	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.53	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.44	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			582	Volts	Peak Drain Voltage is highly dependent on Transformer capacitance and leakage inductance. Please verify this on the bench and ensure that it is below 650 V to allow some margin for transformer variation.
PIVS			27	Volts	Output Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			5.5	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			1.560	Amps	Output DC Current
PO1			8.58	Watts	Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			8.00		Output Winding Number of Turns
ISRMS1			2.946	Amps	Output Winding RMS Current
IRIPPLE1			2.50	Amps	Output Capacitor RMS Ripple Current
PIVS1			27	Volts	Output Rectifier Maximum Peak Inverse Voltage
Pre-Load Resistor			2	k-Ohms	Recommended value of pre-load resistor
CMS1			589	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			22	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.65	mm	Minimum Bare Conductor Diameter
ODS1			1.53	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.93		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2				AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2				mm	Minimum Bare Conductor Diameter
ODS2				mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.93		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils



AWGS3				AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3				mm	Minimum Bare Conductor Diameter
ODS3				mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			8.58	Watts	Total Output Power
Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Note: The spreadsheet shows a warning for the output power parameter “PO” since this value exceeds the maximum output power as specified in the datasheet power table. As indicated in the power table, the power capability is dependent on ambient temperature and the choice of heat sink, etc.

The spreadsheet uses power slightly in excess of 8 W only to achieve sufficient margin for the design. The DER-417 board design is for 8 W application and so the LNK576 part is still being used within the specified rating from the data sheet power table. No device ratings such as peak drain current or peak drain voltage are violated.



9 Performance Data

All measurements performed at room temperature.

9.1 Efficiency at Full Load

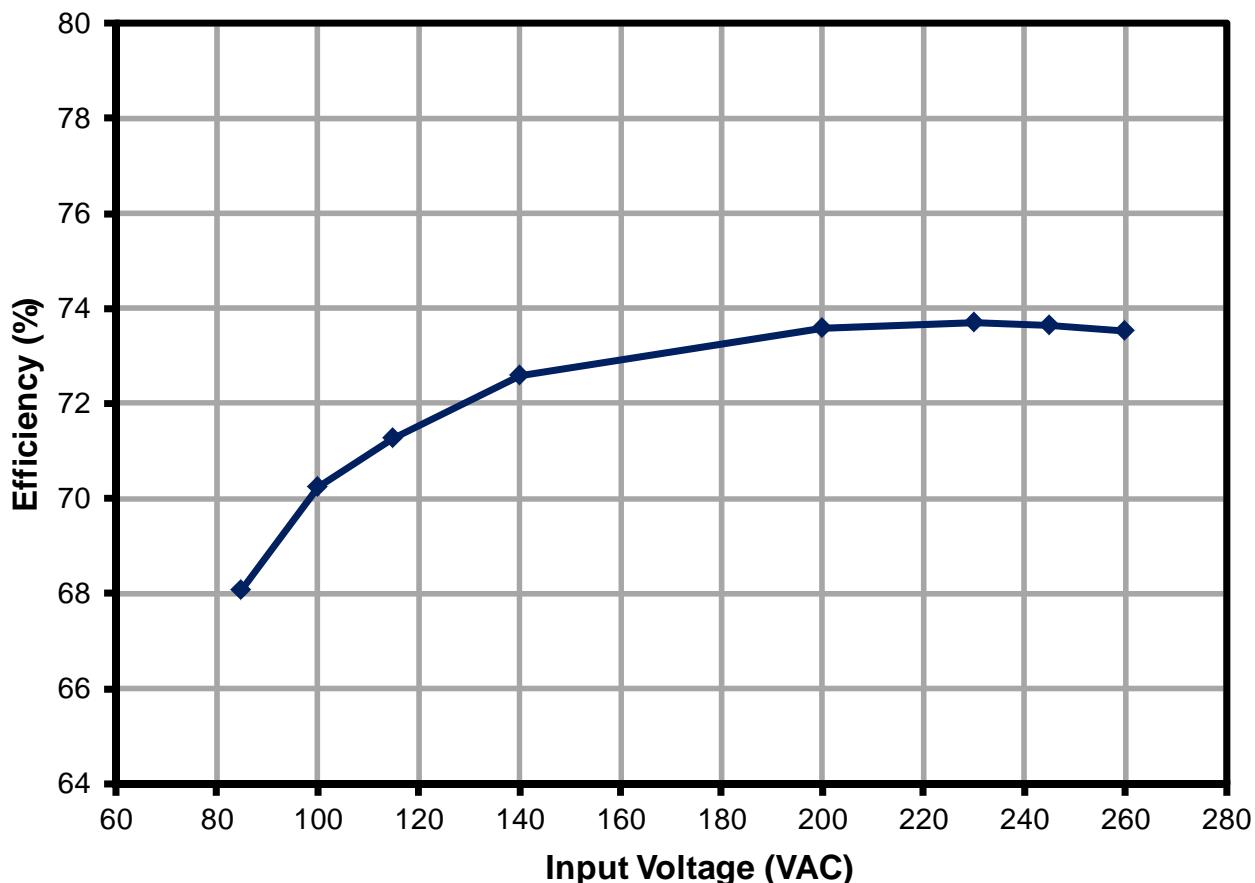


Figure 6 – Efficiency at full load vs. Input Voltage. Room Temperature.

9.2 Average Efficiency

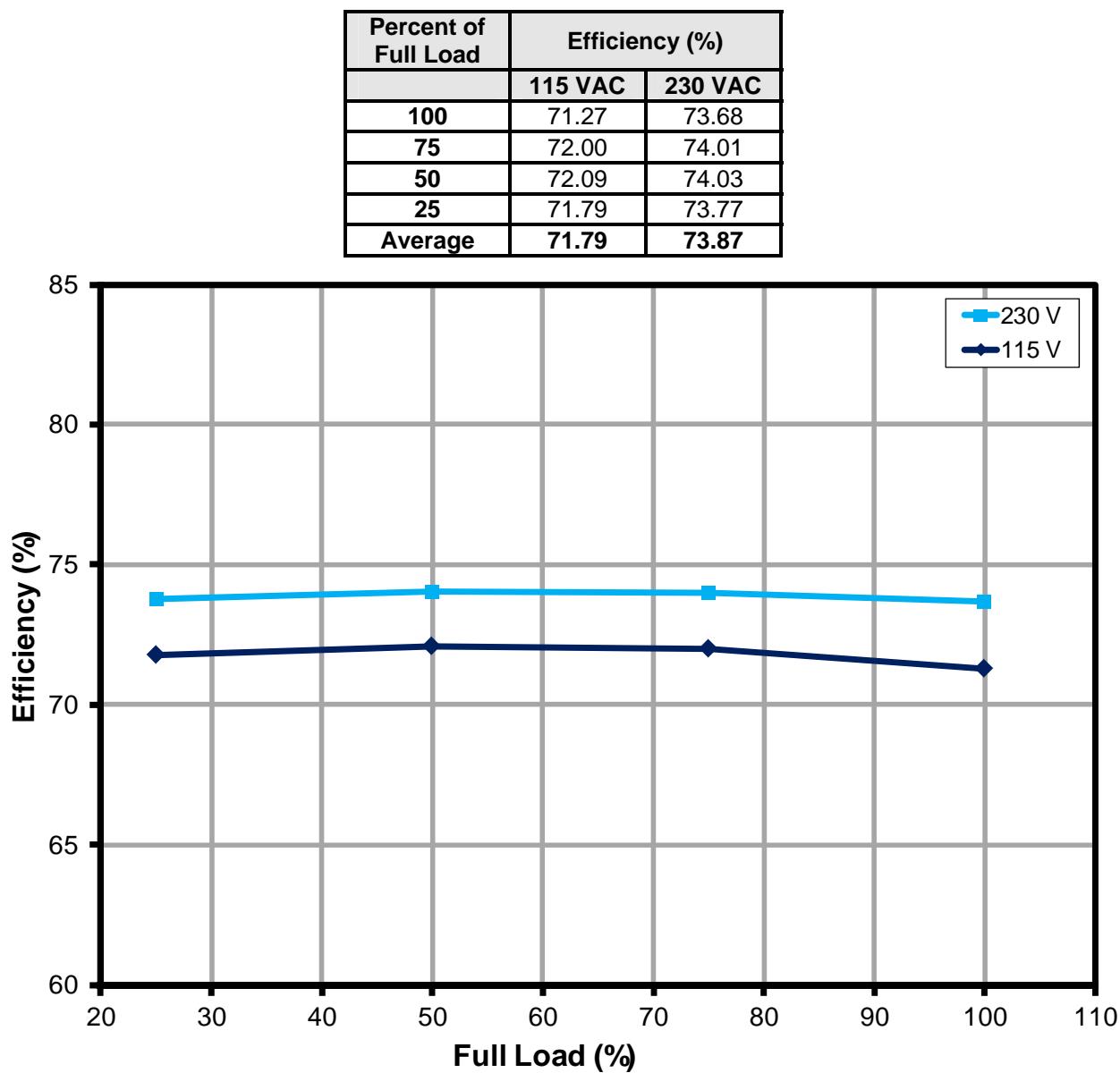


Figure 7 – Average Efficiency vs. Input Voltage. Room Temperature.



9.3 Input Power with 1 mW Output Load

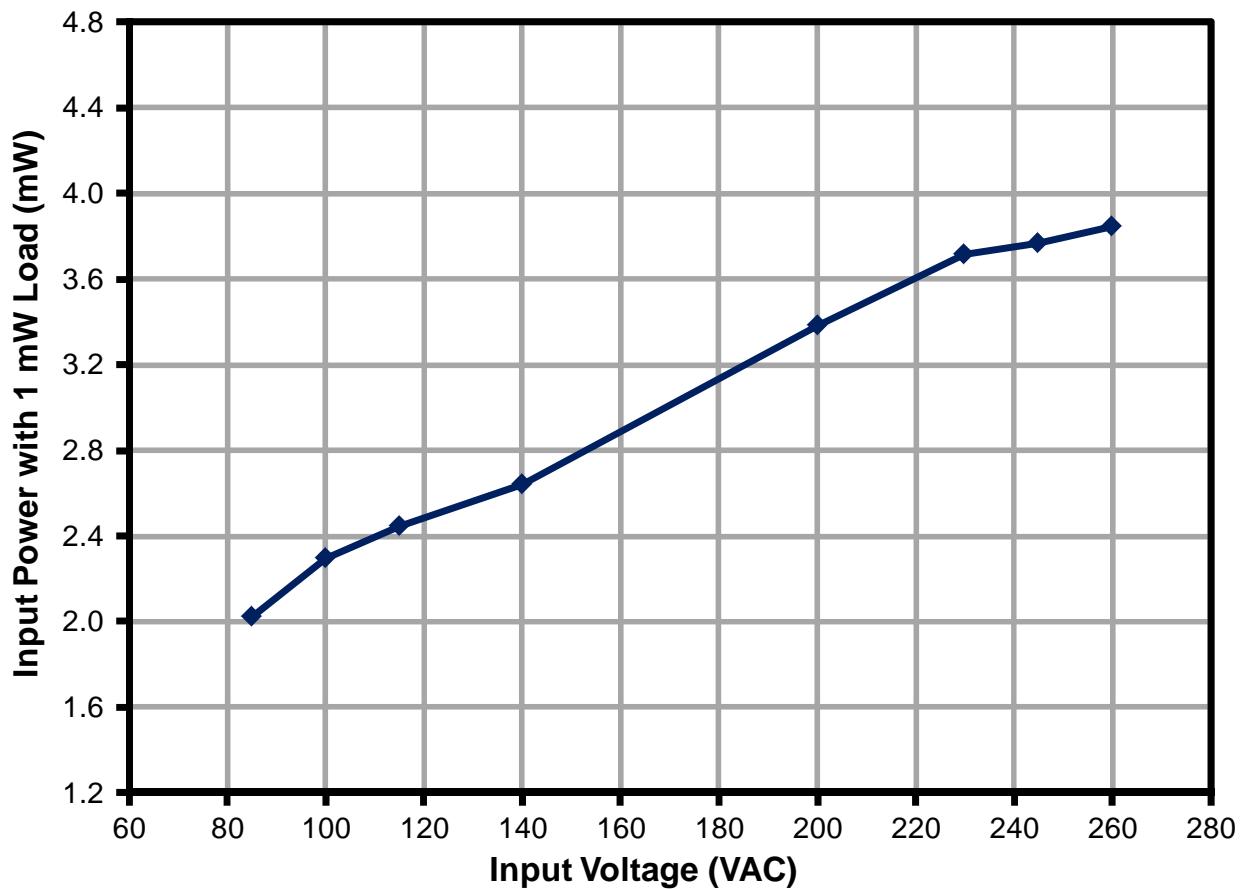


Figure 8 – 1 mW Output Load vs. Input Line Voltage. Room Temperature.

Data measured using a Yokogawa Model WT210 Digital Power Meter.



9.4 Available Standby Output Power

The chart below shows the available output power vs. line voltage for an input power of 0.3 W, 0.5 W, 1 W and 2 W.

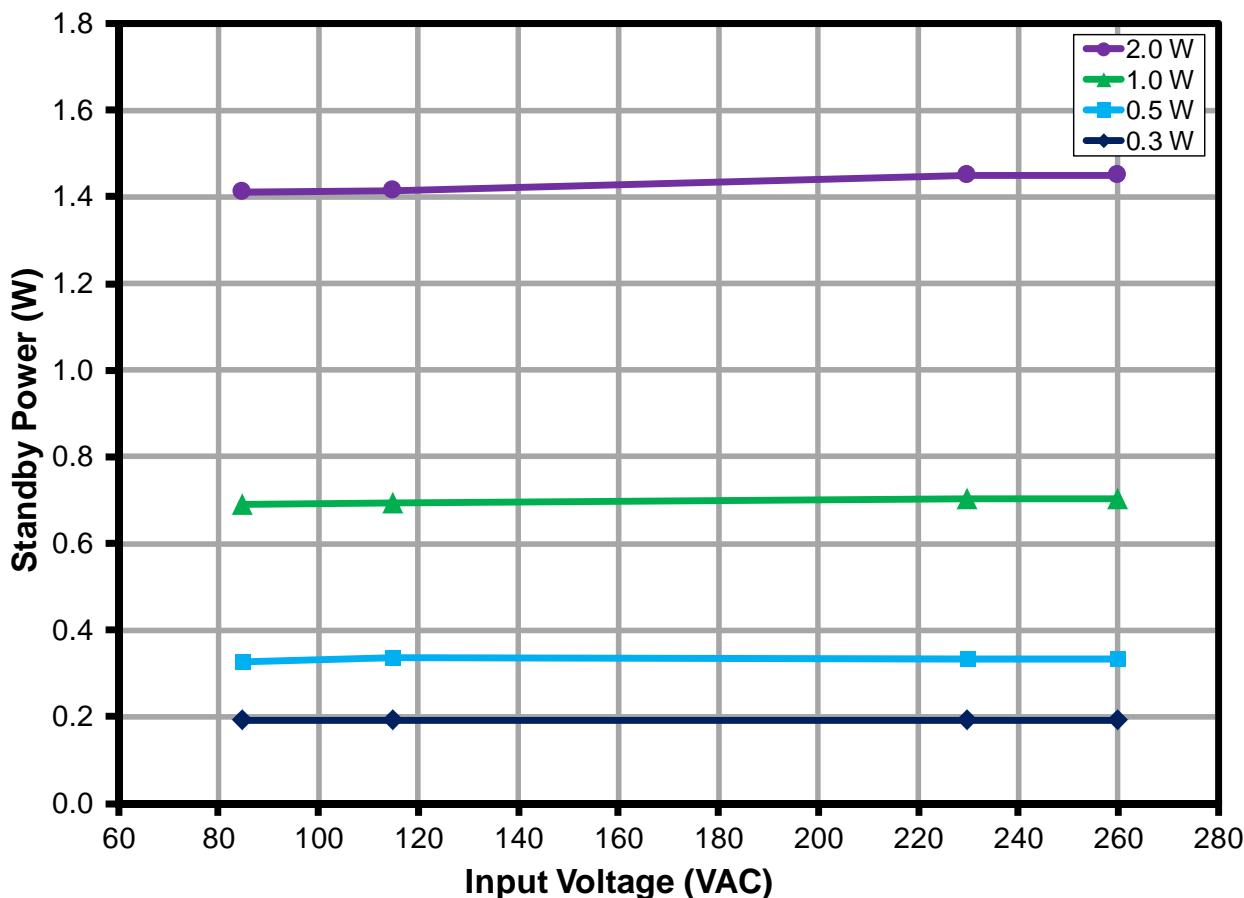


Figure 9 – Available Output Power for 0.2 W, 0.5 W, 1 W and 2 W Input Power Levels.

9.5 Line and Load Regulation

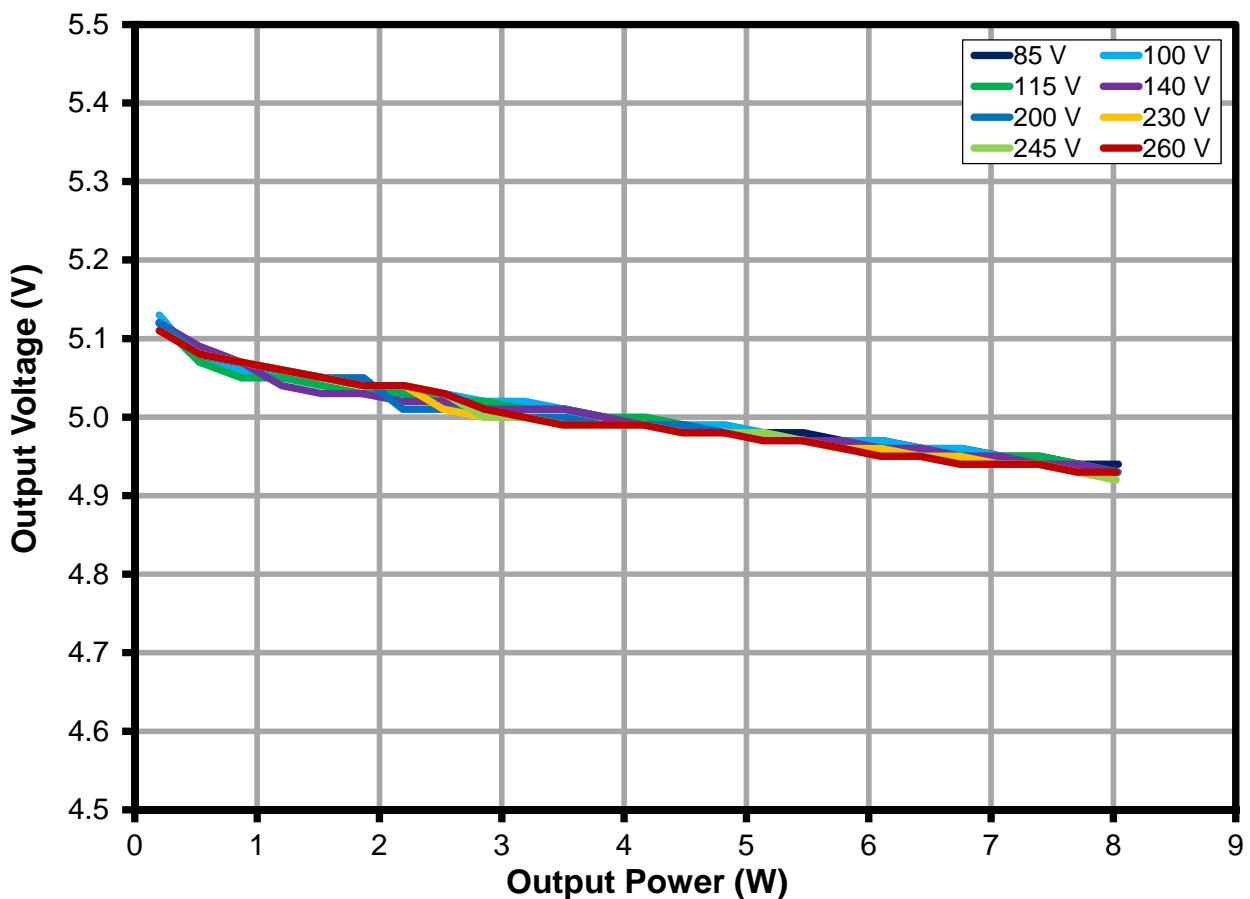


Figure 10 – Load and Line Regulation. Room Temperature.

10 Thermal Performance

10.1 Temperature for 8 W Output and 90 V_{IN}



Figure 11 – 90 VAC, Full Load.
Ambient = 22.8 °C.
LNK576DG = 88.3 °C.



Figure 12 – 90 VAC, Full Load.
Ambient = 22.8 °C.
Transformer = 65.7 °C.
Rectifier Diode = 74.6°C.

10.2 Temperature for 8 W Output and 260 V_{IN}

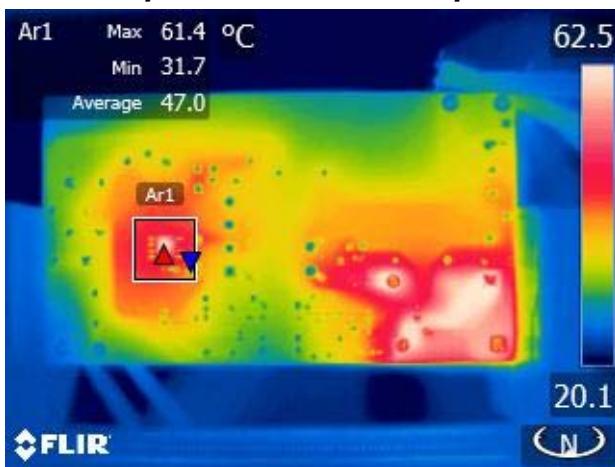


Figure 13 – 260 VAC, Full Load.
Ambient = 23.2 °C.
LNK576DG = 61.4 °C.



Figure 14 – 260 VAC, Full Load.
Ambient = 23.2 °C.
Transformer = 46.0 °C.
Rectifier Diode = 73.8°C.



11 Waveforms

11.1 Drain Voltage, Normal Operation

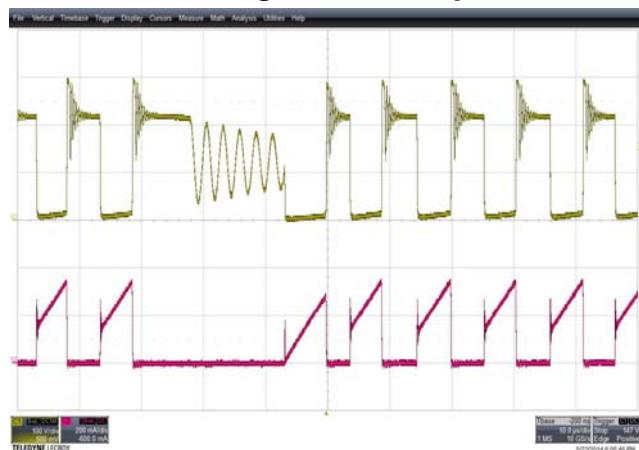


Figure 15 – 85 VAC, Full Load.

V_{DRAIN} , 100 V / div. 10 μ s / div.
 I_{DRAIN} , 200 mA / div.

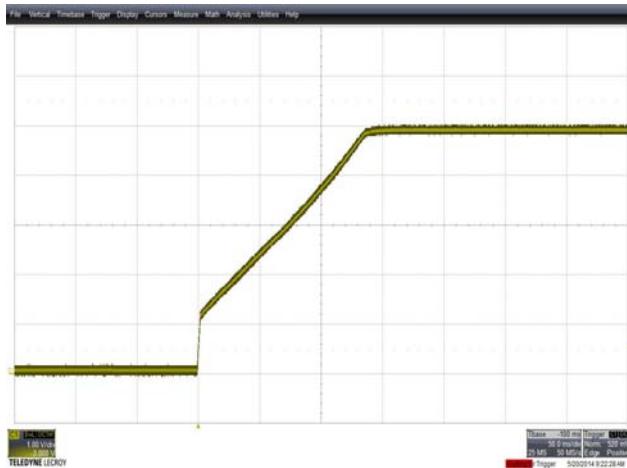


Figure 16 – 260 VAC, Full Load.

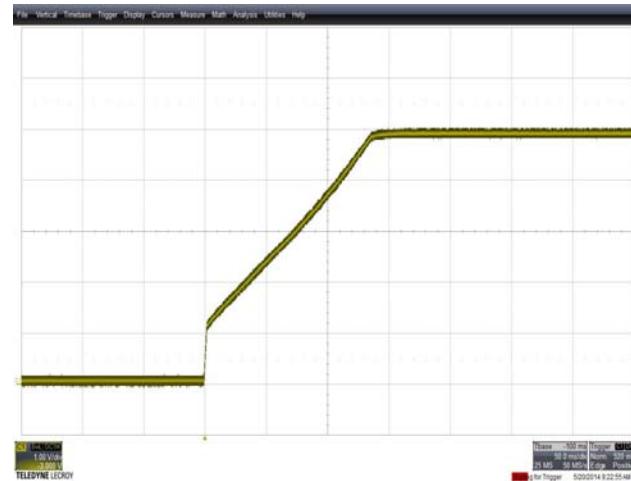
V_{DRAIN} , 200 V / div. 10 μ s / div.
 I_{DRAIN} , 200 mA / div.



11.2 Output Voltage Start-Up Profiles



**Figure 17 – Start-Up Profile, 85 VAC. Full Load.
1 V / div., 50 ms / div.**



**Figure 18 – Start-Up Profile, 115 VAC. Full Load.
1 V / div., 50 ms / div.**



**Figure 19 – Start-Up Profile, 230 VAC. Full Load.
1 V / div., 50 ms / div.**



**Figure 20 – Start-Up Profile, 260 VAC. Full Load.
1 V / div., 50 ms / div**

Using Chroma 6314A/63103A 100 mA / μ s slew rate
Using LeCroy 606Zi at 20 Mhz bandwidth



11.3 Load Transient Response

11.3.1 Transient Response Half Load to Full Load

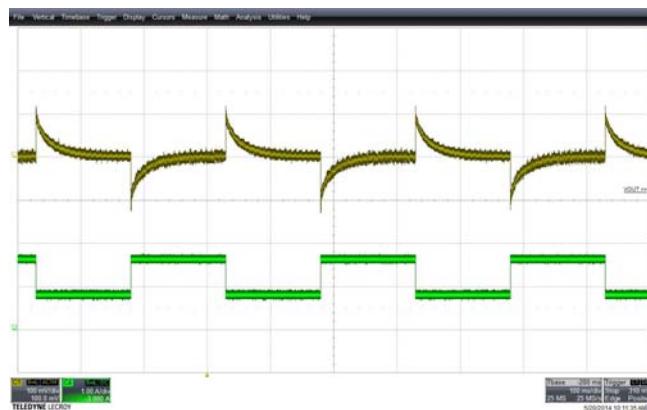


Figure 21 – Transient Response, 85 VAC,
800 mA to 1600 mA. 100 ms / div.
Upper: V_{OUT} 100 mV / div.
Lower: I_{OUT} 1 A / div.

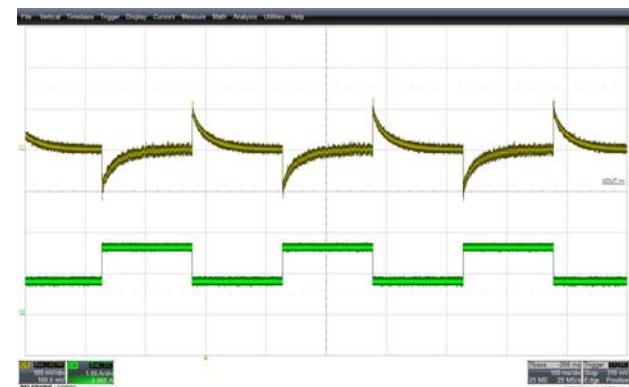


Figure 22 – Transient Response, 115 VAC,
800 mA to 1600 mA. 100 ms / div.
Upper: V_{OUT} 100 mV / div.
Lower: I_{OUT} 1 A / div.

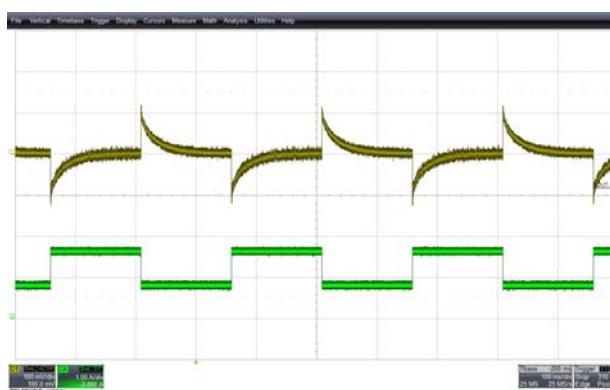


Figure 23 – Transient Response, 230 VAC,
800 mA to 1600 mA. 100 ms / div.
Upper: V_{OUT} 100 mV / div.
Lower: I_{OUT} 1 A / div.

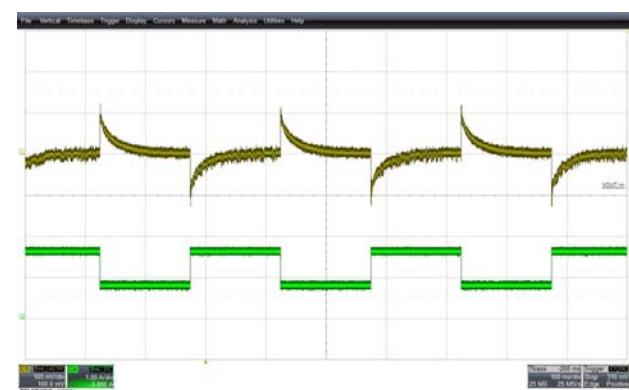


Figure 24 – Transient Response, 260 VAC,
800 mA to 1600 mA. 100 ms / div.
Upper: V_{OUT} 100 mV / div.
Lower: I_{OUT} 1 A / div.

Using Chroma 6314A/63103A 100 mA / μ s slew rate
Using LeCroy 606Zi at 20 Mhz bandwidth



11.3.2 Transient Response 50 mA Load to Full Load

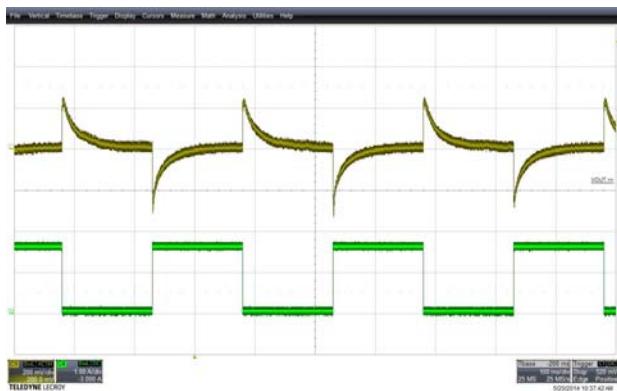


Figure 25 – Transient Response, 85 VAC,
50 mA to 1600 mA. 100 ms / div.
Upper: V_{OUT} 200 mV / div.
Lower: I_{OUT} 1 A / div.

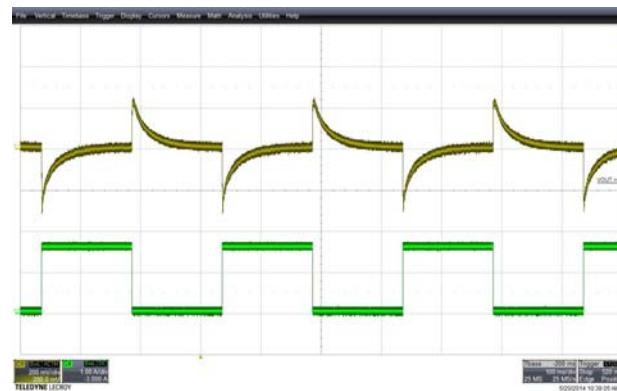


Figure 26 – Transient Response, 115 VAC,
50 mA to 1600 mA. 100 ms / div.
Upper: V_{OUT} 200 mV / div.
Lower: I_{OUT} 1 A / div.

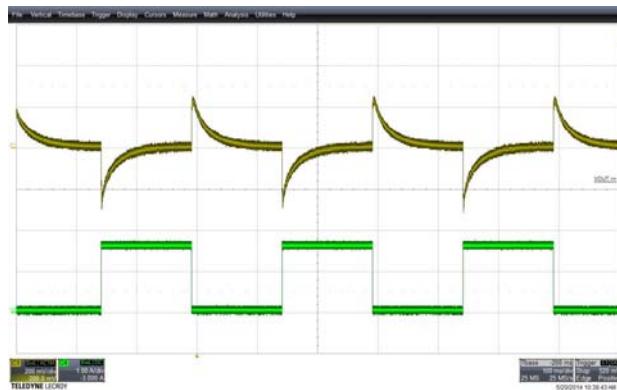


Figure 27 – Transient Response, 230 VAC,
50 mA to 1600 mA. 100 ms / div.
Upper: V_{OUT} 200 mV / div.
Lower: I_{OUT} 1 A / div.

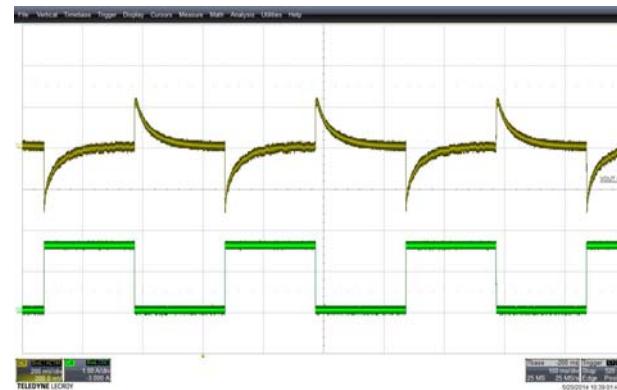


Figure 28 – Transient Response, 260 VAC,
50 mA to 1600 mA. 100 ms / div.
Upper: V_{OUT} 200 mV / div.
Lower: I_{OUT} 1 A / div.

Using Chroma 6314A/63103A 100 mA / μ s slew rate
Using LeCroy 606Zi at 20 Mhz bandwidth

Note: The board can comfortably be loaded to 1.6 A with a load step as fast as 100 mA / μ s as long as a base load of 30 mA is present.



Output Ripple Measurements

11.3.3 Ripple Measurement Technique

A modified oscilloscope test probe was used to take output ripple measurements, in order to reduce the pickup of spurious signals. Using the probe adapter pictured below, the output ripple was measured with a 1 μF electrolytic, and a 0.1 μF ceramic capacitor connected as shown.

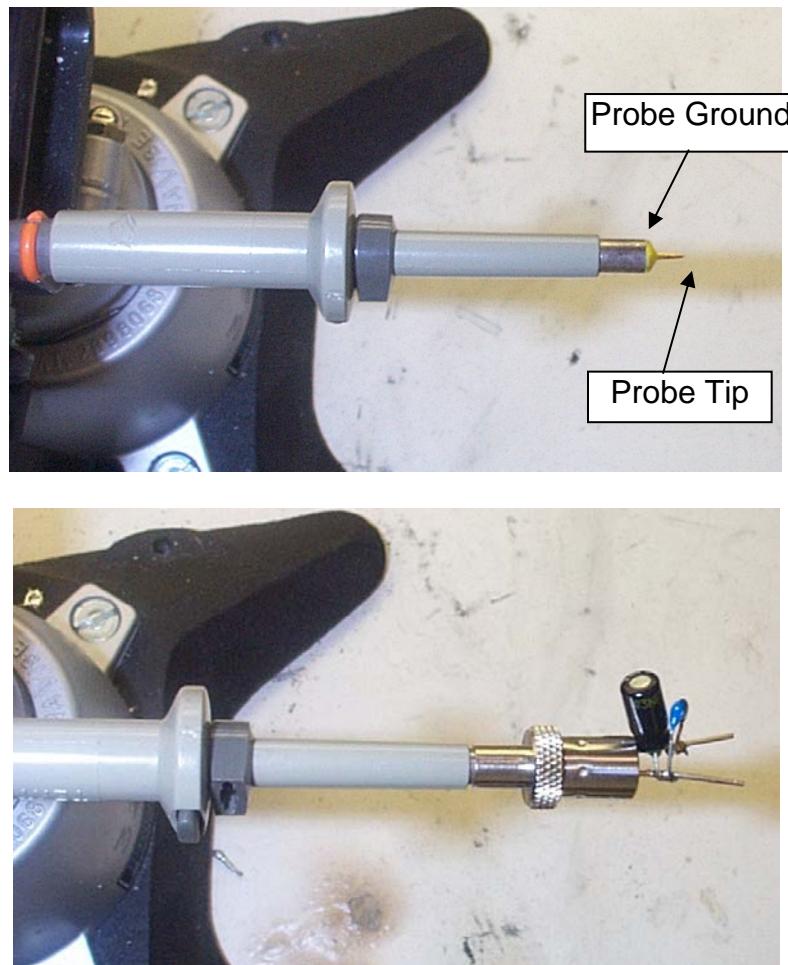


Figure 29 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

11.3.4 8 W Output Ripple Measurements

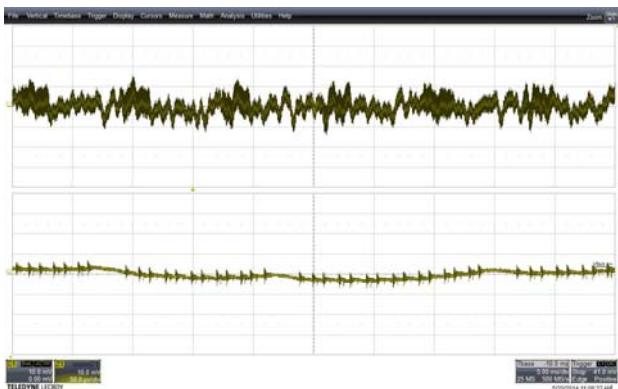


Figure 30 – Ripple, 85 VAC, Full Load.
Upper :5 ms, 10 mV / div.
Lower: 50 μ s, 10 mV / div.

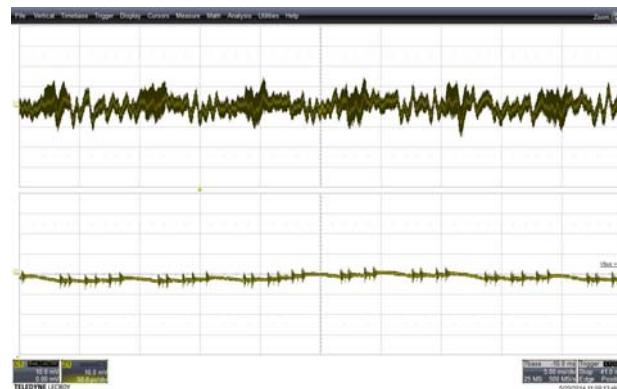


Figure 31 – Ripple, 115 VAC, Full Load.
Upper :5 ms, 10 mV / div.
Lower: 50 μ s, 10 mV / div.

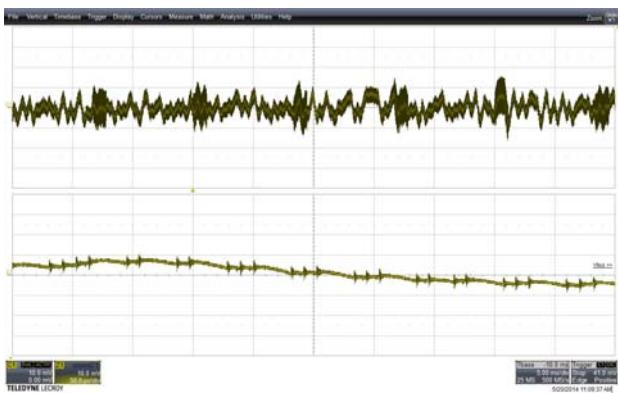


Figure 32 – Ripple, 230 VAC, Full Load.
Upper :5 ms, 10 mV / div.
Lower: 50 μ s, 10 mV / div.

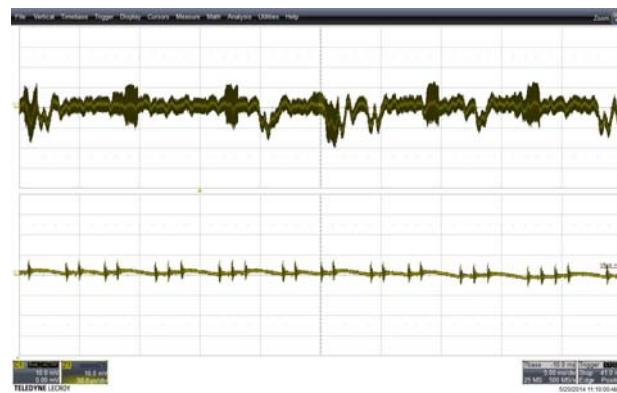


Figure 33 – Ripple, 260 VAC, Full Load.
Upper :5 ms, 10 mV / div.
Lower: 50 μ s, 10 mV / div.

Using Chroma 6314A/63103A
Using LeCroy 606Zi at 20 Mhz bandwidth



11.3.5 Output Ripple Measurements Across Line and Load Range

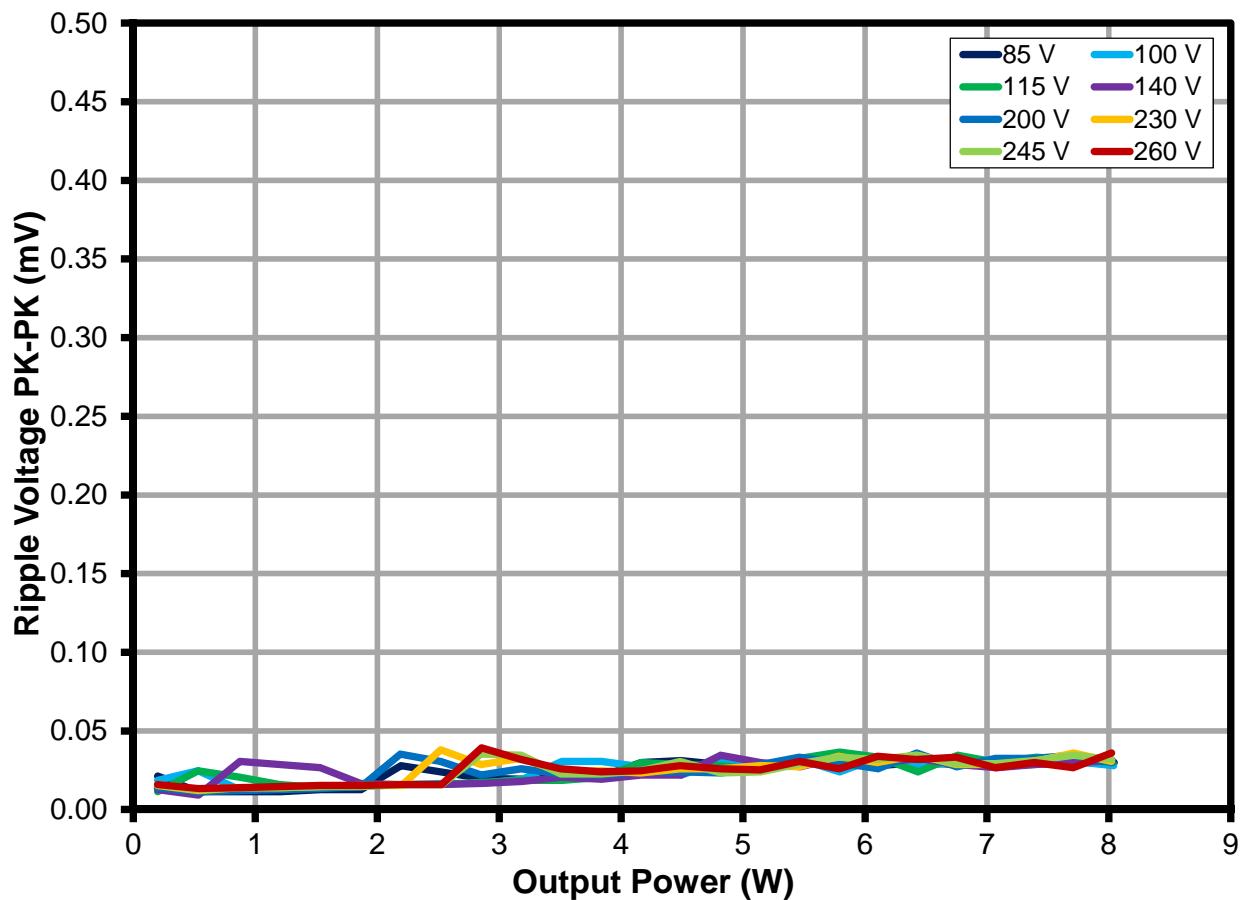


Figure 34 – Output Ripple Voltage Pk-Pk (mV).

Using Chroma 6314A/63103A

Using LeCroy 606Zi at 20 Mhz bandwidth

11.3.6 Output Voltage Ripple with 1 mW Load at 230 V_{IN}

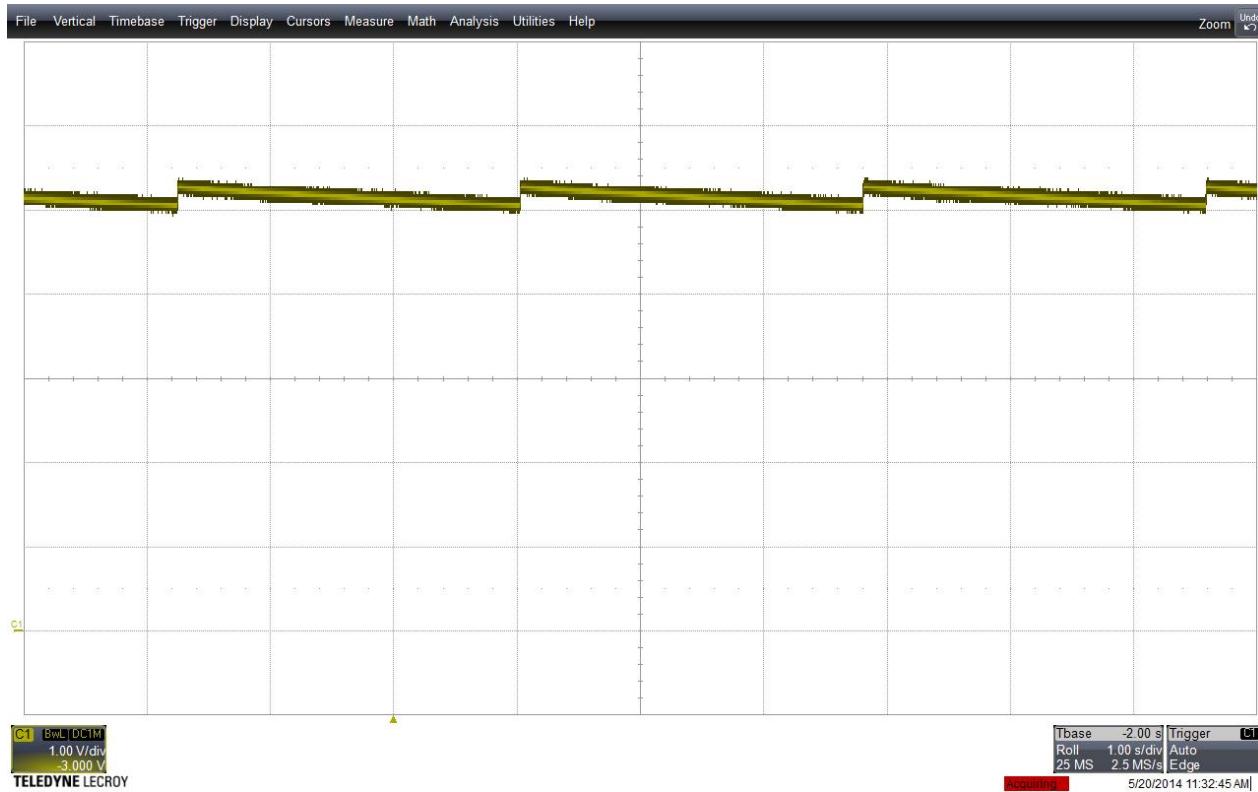


Figure 35 – Time: 1 s / div. Voltage: 1 V / div.

Using Chroma 6314A/63103A

Using LeCroy 606Zi at 20 Mhz bandwidth

Note: The power down voltage ripple voltage can exist for output loads below about 25 mA or 125 mW and the ripple frequency increases with load.

As the load increases above 25 mA the LNK576 will exit the power down mode and the voltage ripple will decrease to normal values.



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12 Revision History

Date	Author	Revision	Description & changes	Reviewed
18-Mar-14	SK	1.0	Initial Release	Apps & Mktg
21-May-14	TM	1.1	Updated Design	Apps & Mktg
25-Jun-14	KM	1.2	Updated Spreadsheet	Apps & Mktg
25-Jun-14	RJ	1.3	Added explanatory note for Spreadsheet	Apps & Mktg



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